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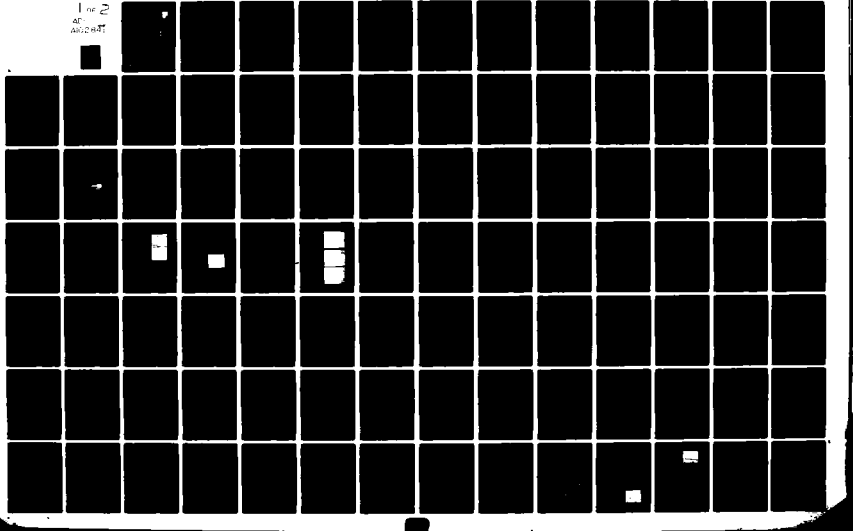

RADC-TR-81-72
Final Technical Report
May 1981

LEVEL II

12

ELECTRICAL CHARACTERIZATION AND SPECIFICATION OF PERIPHERAL DRIVERS, CORE DRIVERS AND MULTIPLYING DACs

General Electric Ordnance Systems

John S. Kulpinski, et al

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

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REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1 REPORT NUMBER: RADC-TR-81-72	2 GOVT ACCESSION NO: AD-A102 847	3 RECIPIENT'S CATALOG NUMBER
4 TITLE (and Subtitle): ELECTRICAL CHARACTERIZATION AND SPECIFICATION OF PERIPHERAL DRIVERS, CORE DRIVERS AND MULTIPLYING DACs	5 TYPE OF REPORT & PERIOD COVERED: Final Technical Report, Jan 80 — Jan 81
	6 PERFORMING ORG REPORT NUMBER: N/A
7 AUTHOR(s): John S. Kulpinski, et al.	8 CONTRACT OR GRANT NUMBER(s): F30602-80-C-0057
9 PERFORMING ORGANIZATION NAME AND ADDRESS: General Electric Ordnance Systems, Electronic Systems Division, Pittsfield MA 01201	10 PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 62702F, 23380186
11 CONTROLLING OFFICE NAME AND ADDRESS: Rome Air Development Center (EBRA), Griffiss AFB NY 13441	12 REPORT DATE: May 1981
	13 NUMBER OF PAGES: 120
14 MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): Same	15 SECURITY CLASS (of this report): UNCLASSIFIED
	15a DECLASSIFICATION/DOWNGRADING SCHEDULE: N/A

16 DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17 DISTRIBUTION STATEMENT (of the abstract ente

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19 KEY WORDS (Continue on reverse side if necessary and identify by block number)

Reliability
Interface Microcircuit
Characterization

20 ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report covers the work performed by General Electric Ordnance Systems Division pertaining to the electrical characterization and specification of interface types of microcircuits. The period of report is January 1980 to January 1981. The main thrust of this electrical characterization effort was directed at high military usage peripheral and core drivers and multiplying CMOS digital to analog converters. The

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following device types were evaluated:

Peripheral Drivers - 55450 and 55460 family,

Core Drivers - 55325/6/7, and

Multiplying CMOS DACs - 7520 family.

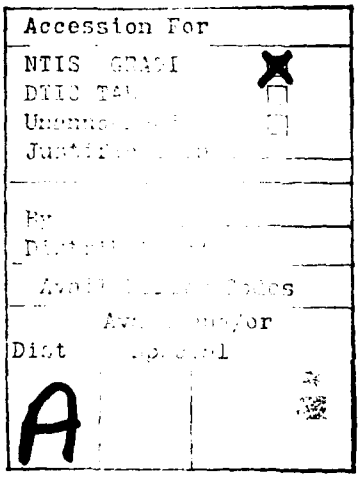
Data obtained during device characterization is published in handbook form and is available under separate cover from this document. However, samples of data sheets, histograms and plots are included in this report.

PREFACE

This report was prepared by General Electric Ordnance Systems, 100 Plastics Avenue, Pittsfield, Massachusetts, for Rome Air Development Center, Griffiss Air Force Base, Rome, New York, under contract F30602-80-C-0057. It covers the period from January 1980 to January 1981.

The work on this project was performed by the Electronic Circuits Engineering Operation of Ordnance Systems. Project responsibility was held by Mr. John Kulpinski of Circuit Design Engineering. Key individuals who made significant contributions to this work effort were Messrs. Thomas Hack and Theodore Simonsen of Circuit Design Engineering and Messrs. Larry Deluca, John Dunn, Robert Mossman and Jamie Schwehr of Circuit Test Engineering.

Mr. Thomas Dellecave, RBRA, is the Project Engineer at RADC for this contract.



ELECTRICAL CHARACTERIZATION AND SPECIFICATION OF
PERIPHERAL DRIVERS, CORE DRIVERS, AND MULTIPLYING DACs

List of Sections

SECTION I

INTRODUCTION

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SECTION I

INTRODUCTION

Objectives

The overall objective of this work effort is to characterize and specify MIL-M-38510 ("General Specification for Microcircuits") detailed slash sheets.

Generally, "characterization" of a device type includes several related tasks:

- o Assessment of test parameters, limits, and test conditions.
- o Development of test procedures and test circuits compatible with automatic test systems.
- o Analysis of limits and verification of test circuits via sample device testing and data evaluation.
- o Assessment of device performance, identification of anomolies.
- o Generation and verification of detailed burn-in life test circuits

Concurrent with characterization, detailed MIL-M-38510 slash sheet development includes:

- o Formulation of Table I, Electrical Performance Characteristics selection of test parameters required by military users and determination of test conditions and limits, compatible with automatic test methods and with device yield.
- o Formulation of Table II, Electrical Test Requirements; Table III, Group A Inspection; Table IV, Group C End Point Electrical parameters.
- o Design of static and dynamic test circuits, terminal connection diagrams, steady-state power and reverse bias burn-in circuits, accelerated burn-in and life test circuits.

All of the above activity is either guided by or reviewed by the manufacturers of the devices involved, and by Rome Air Development Center (RADC).

All of the characterization and specification effort performed is based upon the fundamental objectives of the JAN 38510 program - namely quality, reliability, interchangeability, and standardization.

Scope of Applied Effort

The specific tasks included in this effort are the characterization and specification of the following generic device types:

- o Peripheral Drivers
- o Core Drivers
- o Multiplying DACs

Originally, sense amplifiers and line drivers were also planned for characterization. Lack of vendor interest and support plus discontinued production by one vendor, led to cancellation of that effort and addition of the multiplying DAC effort.

Background

General Electric Ordnance Systems, one of 166 operating product departments of the General Electric Company, develops and produces precision electromechanical and electronic military systems. Current activities include development, design and production of fire control and guidance systems for the Navy's TRIDENT Fleet Ballistic Missile program, the MK 73 Gun and Guided Missile Director (TARTAR), the MK 80 Director (AEGIS), the PHALANX close-in weapon system, MK 45 Gun Mounts, turret drive and stabilization systems for the Army's Infantry Fighting Vehicle, advanced torpedo propulsion, and jet engine controls.

As users of microcircuits for military systems, Ordnance Systems has also performed electrical characterization of certain linear, digital, and interface microcircuits for MIL-M-38510 specification under previous contracts to Rome Air Development Center. These specification acitivities date back to 1971 and include seventeen separate contracts.

General Electric began this current effort in MIL-M-38510 microcircuits on January of 1980, having previously completed similar characterization and specification contracts in 1976 - 1979. Philosophies for establishing parameters, limits, and test circuits for conventional devices like op amps, comparators, logic devices and data converters were developed and coordinated with RADC, DESC, and the device manufacturers.

This current effort extended past efforts to a new class of devices, peripheral drivers and memory core drivers, and thus established important groundwork in the development of automatic tests and specifications for high-speed, high-voltage/current logic drivers.

Currently there are approximately thirty completed and in-process linear/interface slash sheets in the MIL-M-38510 program. Six slash sheets are devoted to op amps including the bipolar "standards", followers, BIFETs, quads, high-slew-rate, and lo-power and lo-noise BIFETs. Comparators, transistor arrays, and precision timers are contained in four slash sheets, as are CMOS and JFET analog switches. Voltage regulators are specified in six

separate slash sheets, and precision voltage reference in two others. Three slash sheets are devoted to D/A converters, and one each to A/D converters, sample/hold circuits, peripheral drivers, memory core drivers, and line drivers and line receivers.

Development of Slash Sheets

A procedure for developing new slash sheets to MIL-M-38510 has evolved through negotiations among all concerned parties. Device selection is influenced by user needs, which is determined from the marketplace and from organized committees, such as the Military Parts Control Group (MPCAG) at DESC, the G12 Solid State EIA Device Committee, and the Microelectronics Project Group of the Electronics Systems Committee of AIA. These recommendations are balanced with manufacturer recommendations obtained via the JC-41 Committee on Linear Microcircuits. Devices of recent vintage, having high usage, multiple application potential in military systems, proven performance, and two or more sources are given priority. Single-sourced devices are acceptable, especially for hybrid devices, although multiple sources are preferred. Availability of devices, and expressed manufacturer interest in supporting slash sheet development are additional important considerations. Manufacturers typically recommend devices for slash sheet action in JC-41 Committees, and then chair a JC-41 Subcommittee for preparation of slash sheet parameters, limits, and test circuits.

The industry data sheet forms the basis for the military specification parameters and limits. Typically, such data sheets do not specify all of the necessary parameters over the military temperature range and over the common mode voltage range. The JC-41 Subcommittee, or the device manufacturer, usually prepares a proposed spec which contains more information than the industry data sheet. Conflicting items are negotiated in committees or via direct contact with manufacturers.

Data provides another base for determining parameters and limits. Devices for test are purchased from distributors and are also obtained from manufacturers via RADC request. Test circuits, compatible with automatic test systems, are developed. The devices are tested on a Tektronix S3263 Automatic Test System at GE Ordnance Systems Electronic Test Center. Data obtained at -55°C, +25°C, and + 125°C ambient is correlated to bench or vendor test data, analyzed, reduced and documented in data handbooks. Recommended limits are compared to the statistical sample data; parameter limits which are grossly inconsistent with the data are readily identified.

Specification additions, changes, and alternate approaches are discussed at the committee level. Device anomalies are identified in lab bench tests. Failure modes are also identified. User caution notes are added to the specification if it is deemed appropriate.

Burn-in circuits are usually recommended by the manufacturer and evaluated by RADC and/or GEOS on the available test samples. An objective is to minimize the number of external components while stressing the device near its limits.

Rough draft copies of the final slash sheet are prepared at GEOS and are forwarded to RADC for review. DESC distributes copies of this spec to manufacturers and users for final comments. Following assessment of the comments by all concerned parties, DESC prepares and issues the slash sheet.

Characterization Data

Data obtained during device characterization is usually published in handbook form separate from this document. Samples of the data sheets, histograms, and plots, are included in this report. The following data handbooks were published during this contract effort:

Characterization Data for MIL-M-38510/129, Peripheral Drivers
(Commercial Types 55450 - 454, 55460 - 464) Jan 81

Characterization Data for MIL-M-38510/127, CMOS Multiplying DACs
(Commercial Types 7520, 7521, 7523, 7541) Jan 81

Formal Meetings Attended (GE internal meetings not included)

JC-41 Committee on Linear ICs

Feb. 5, 6, 1980	-	Phoenix, AZ
June 10, 11, 1980	-	Washington, DC
Oct. 7, 8, 1980	-	Burlington, MA

RADC/GE Meetings

Jan. 25, 1980	Contract Plans	Pittsfield, MA
Mar. 4, 1980	Contract Status & Plans	Rome, NY
Aug. 13, 1980		

SECTION II

AUTOMATIC TEST DEVELOPMENT

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SECTION II
AUTOMATIC TEST DEVELOPMENT

2.1 Introduction

The Interface Microcircuits & linear characterization efforts required the accumulation and subsequent reduction of vast amounts of test data. For both of these tasks, GE made extensive use of a Tektronix S-3270 test system and a Tektronix software development system. This section will describe the test system and the general approach to expanding its capabilities. A few displays of raw and of reduced data, which have been developed for the device evaluations, will also be shown. Although several of the data displays are somewhat standardized, many of the linear device types required the development of unique data displays in order to effectively illustrate device performance in an easily digestible form.

2.2 Tektronix S-3270 Test System Features

The test system is fully equipped to provide a state-of-the-art engineering tool for device characterization. The CP1162 System Controller has the Date/Time Option that gives the ability to store date and time information in the directory and data files. System peripherals include a 4014 Graphics Display Terminal, two CP110 Disk Drives, a CP220 Reader/Punch, and LA180 Decprinter I and a 4631 Hard Copy Unit.

For voltage and current measurement and device stimulation, the system contains:

1304 Test Station, which contains many test functions and all electronics to interface the device under test (DUT) to the system.

2943/44 Clock Generators, which provide 10 driving and 4 comparing programmable phases.
Option 20 Waveform Digitizer, which provides the capability of converting 1000 points on a waveform to 10-bit digital values.

Once the waveform is thus stored in memory, software can be used to determine such things as rise time, overshoot, settling time, etc.

Six programmable voltage sources.

Two programmable current sources.

Temptronix 450A Temperature Chamber, which allows programmable DUT temperatures from -60 deg C to + 160 deg C.

IEEE Bus Interface Card, which allows the addition of IEEE 488 compatible equipment to the system.

With these hardware components, the test system has the following features:

Accommodates up to 128 active pins (64 input, 64 output)
Functional testing at 20 Mhz; force, compare, mask and store at 20 Mhz

DC Tests: Differential voltage measurements; force V, measure I; force I, measure V

Dynamic Testing: Repetitive and one-shot time measurements; functional preconditioning

GO/NO-GO and analytical test capability

On-line interactive program development

Digital waveform analysis (1 sample/picosecond)

DUT environmental control (-60 deg C to 160 deg C)

Data logging and reduction. Computer graphics display

2.3 Tektronix System Accuracy

The linear test programs were developed to utilize the internal Tektronix measurement/stimulus hardware as much as possible. However, for many measurements, the Tektronix system could not provide the required accuracy. In these cases, more accurate external equipment was utilized via the IEEE 488 Bus. Two disadvantages in using external equipment are:

1) additional core is required to store the 488 bus control routines and,

2) execution time for external functions is significantly longer than time to execute internal Tektronix functions.

Table 2.1 lists instruments which are available for use with the S-3260/70.

Table 2.1 IEEE-488 Interfaced Instruments.

Manufacturer	Model	Description
Fluke	8502A	Precision Digital Multimeter
Hewlett Packard	3455A	Precision Digital Voltmeter
Hewlett Packard	4262A	LCR Meter
Hewlett Packard	5328A	Universal Counter
Fluke	5100A	Calibrator
Kepco	488-122	Power Supply Programmer
ICS Electronics	4880	Instrument Coupler
Hewlett Packard	2240A	Measurement and Control Processor
North Atlantic	225	Phase Angle Voltmeter

Figures 2-1 through 2-13 illustrate the accuracies of the internal Tektronix measurement and stimulus functions. Also, for certain internal functions, the accuracy of the external equipment that provides the same function, is displayed for comparison.

On many occasions, neither the internal Tektronix equipment nor the external equipment had sufficient accuracy, or response time. These cases required test adapter circuitry to interface the device under test (DUT) to the test equipment. These cases will be described in the appropriate chapters covering the individual linear device types.

2.4 Correlation

Testing linear devices on the Tektronix system has required the implementation of many new test techniques. Each new technique, whether in the form of adapter circuitry or software, must be verified as accurate. In general, the first step of verification was to determine that the technique is designed to provide a measurement that is at least 10 to 1 times more accurate than the tolerance of the parameters. For instance a parameter of 5.0 volts plus or minus 10% must be measured by a meter that is at least accurate to plus or minus 1% when measuring 5.0 volts.

Verification of accuracy also included comparison of data taken by the new technique to data taken by an alternate method - usually on a bench circuit. When data from the two techniques did not agree, an analysis of error contributions was performed and corrections made if it was felt that the error was significant.

Correlation of Tektronix test data for peripheral driver devices to bench data uncovered some discrepancies. One discrepancy involved the inaccurate specification of worst case test conditions for output switching times. Correlation uncovered the discrepancy and led to recommended changes to the slash sheet.

2.5 Data Reduction

The presentation of test results is extremely important in any characterization effort. Raw data printouts are required for record, but are usually not organized in a manner that enables one to scan them to assess general parameter trends.

Data Tables

For the linear devices, the first step in data reduction was organizing raw data into tables. Figure 2-14 and 2-15 illustrate two variations of data tables. Figure 2-14 illustrates data taken from multiplying D/A devices. Figure 2-15 is the form of table used for the Peripheral Driver devices. The left hand entries indicate the test parameters and test conditions. In Figure 2-14 the data from a particular device is entered in the column beneath the temperature at which the data was taken. In Figure 2-15, the data taken for five devices at a particular temperature, is entered in columns. Note that in both figures the low test specification limit for each parameter is on the left of the device data and the high specification limit is on the right hand side of the data. This enables the reader to more easily determine if a measurement on a device lies mathamatically between the specification limits.

Data Summaries, Line Graphs

Data tables, for the multiplying D/A with its large number of data points are too voluminous for a reader to mentally reduce and detect trends. Therefore the large quantities of data must also be presented in a summarized form.

Figure 2-16 is a plot of linearity error (in LSBs) for all codes between 0 and 800. The plot is one of five sheets developed for each 7520 multiplying D/A device. The linearity plots were very instrumental in verifying the effectiveness of an abbreviated linearity test for 7520 multiplying D/A devices. Although two seperate sheets were required for each device under each set of operating conditions, one set of sheets allows one to quickly assess qualitatively, the linearity error of 1024 codes.

Histograms

Tektronix software included a basic histogram routine which was modified by GE to provide the variations shown in Figures 2-17 and 2-18. Figure 2-18 has grouped thirty devices according to hFE. The histogram differs from the basic Tektronix histogram in that the bars are filled in and are separated by a narrow non-darkened region. Figure 2-18, another histogram variation, groups the codes from a single multiplying D/A device, according to the magnitude of each code's error. This type of plot is very useful in comparing general linearity error characteristics of one device to another.

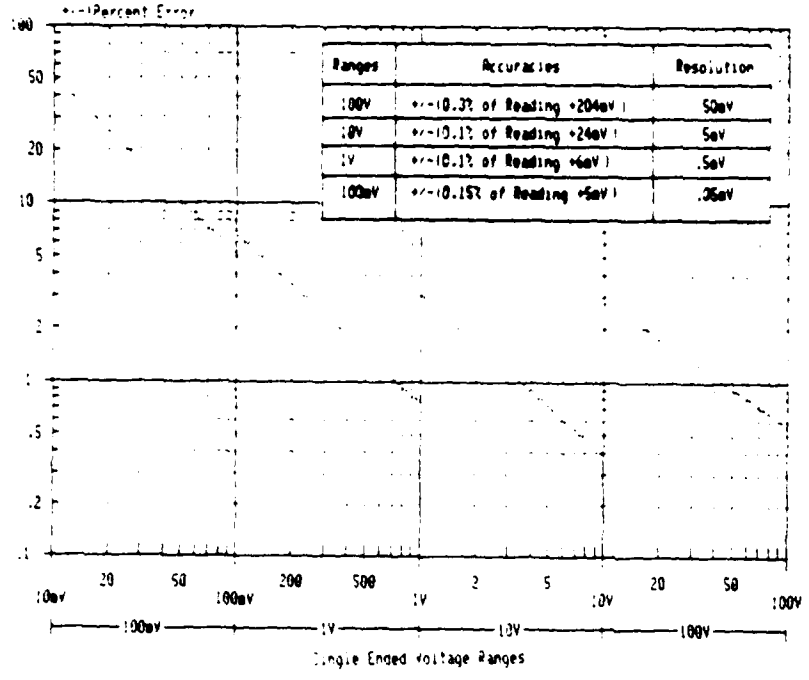


Figure 2-1. 3320/70 - Single Ended Voltage Accuracies

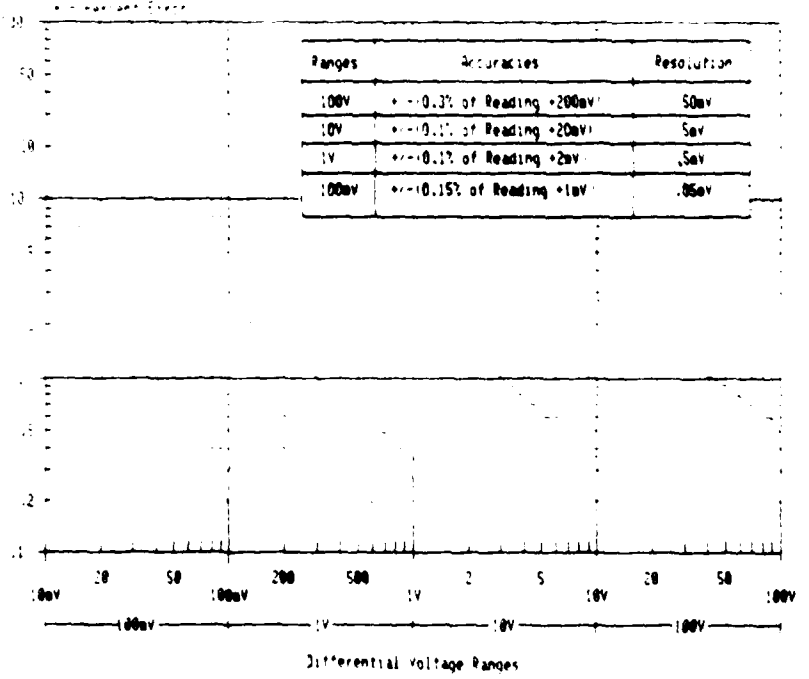


Figure 2-2. 3320/70 - Differential Voltage Accuracies

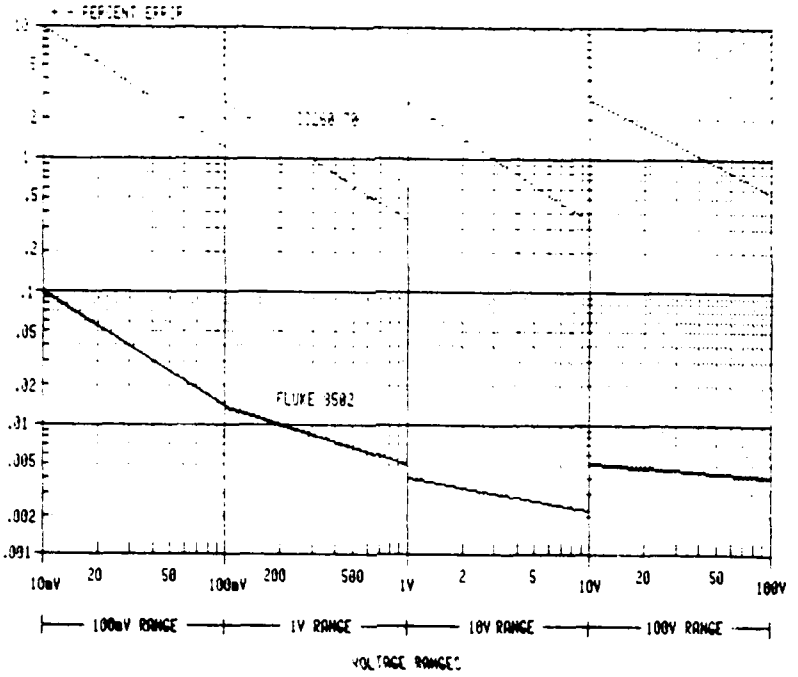


Figure 2-3a. S3260/70 - Diff. Meas. vs. Fluke 8502 DVM Accuracies

FLUKE DMM 8502A

Range	Full Scale	Accuracies	Resolution	Settling Time
100mV	312mV	0.005% of Reading +3uV	1uV	2mS
1V	2.5V	0.004% of Reading +9uV	1uV	2mS
10V	20V	0.002% of Reading +90uV	10uV	2mS
100V	160V	0.004% of Reading +900uV	100uV	2mS

TEKTRONIX S3260/70
DIFF. VOLTAGE MEASUREMENTS

Range	Full Scale	Accuracies	Resolution	Settling Time
100mV	102.2mV	+/-(0.15% of Reading+1mV)	0.05mV	4mS
1V	1.022V	+/-(0.1% of Reading+2mV)	0.5mV	.6mS
10V	10.22V	+/-(0.1% of Reading+5mV)	5mV	.6mS
100V	102.2V	+/-(0.3% of Reading+200mV)	50mV	1.2mS

Figure 2-3b. S3260/70 - 8502 DVM Specification Comparison

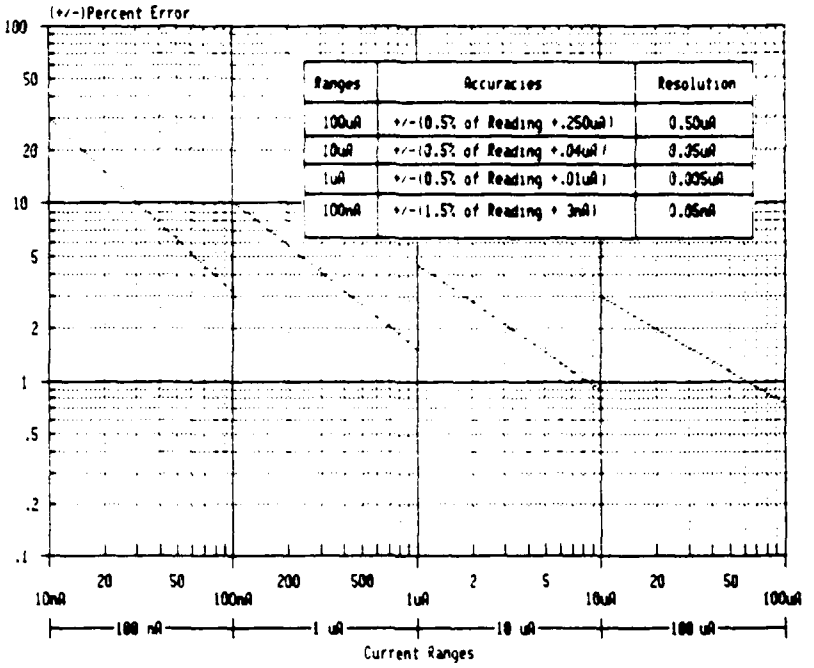


Figure 2-4. S3260/70 - Current Measurement Accuracies

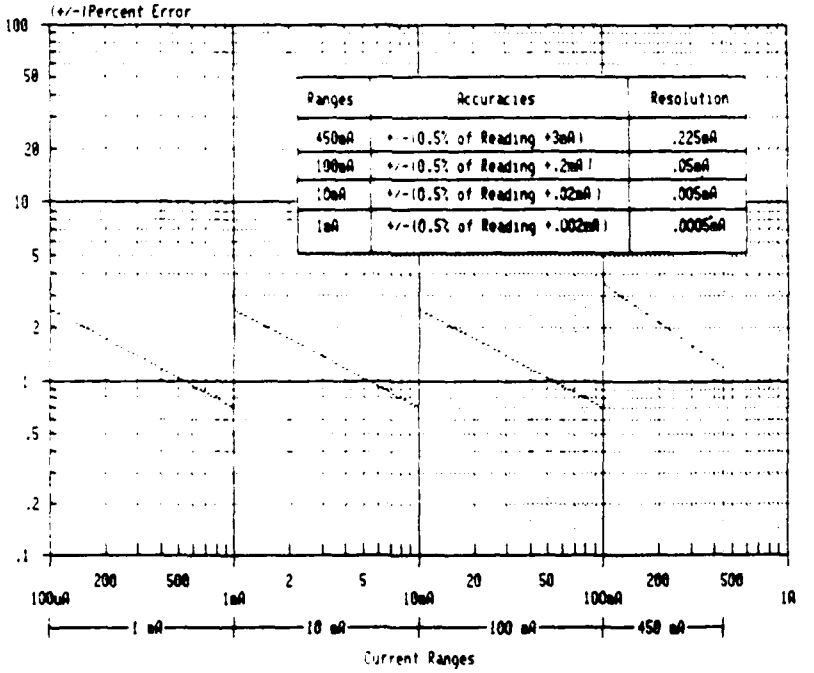


Figure 2-5. S3260/70 - Current Measurement Accuracies (Cont'd.)

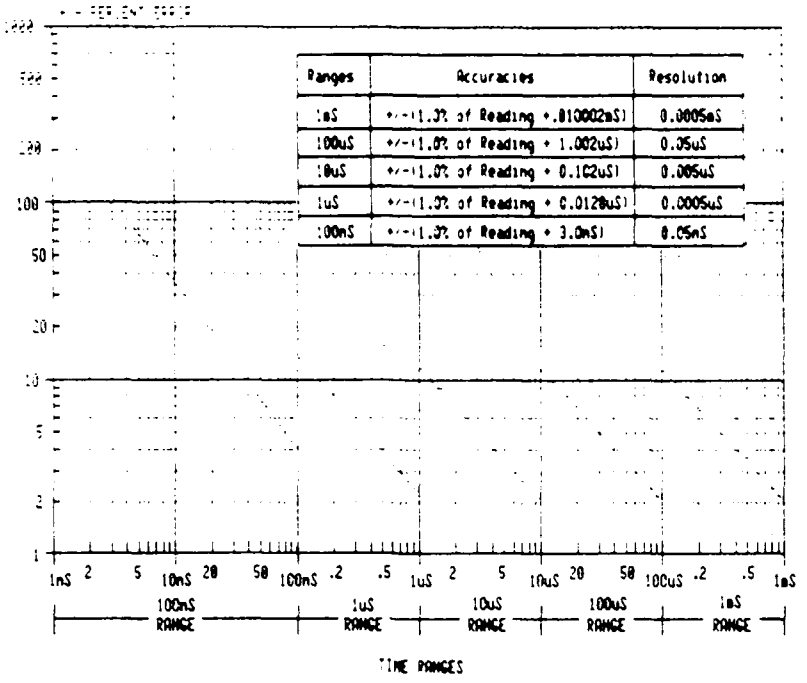


Figure 2-6. S3260/70 - Time Measurement Accuracies

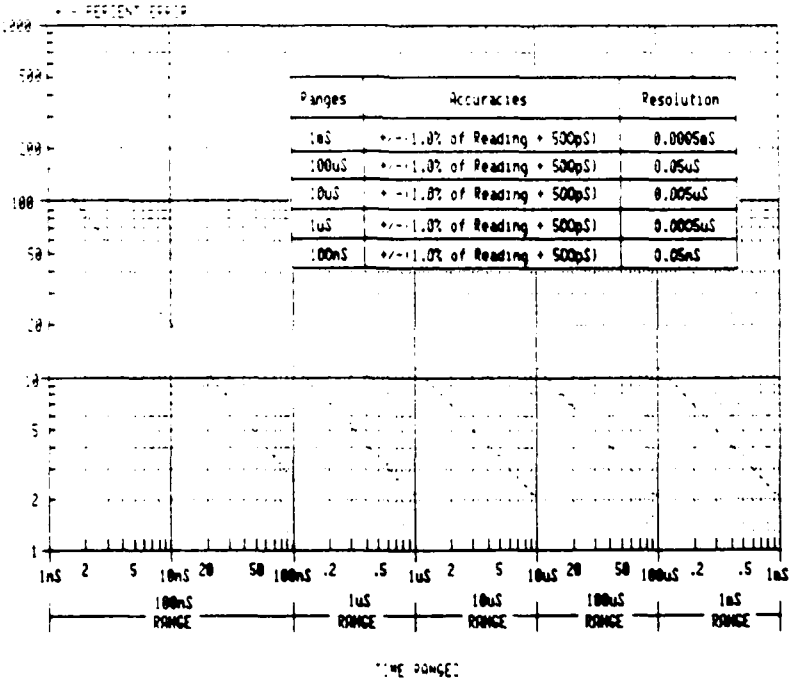


Figure 2-7. S3260/70 - Time Measurement Accuracies - HPO

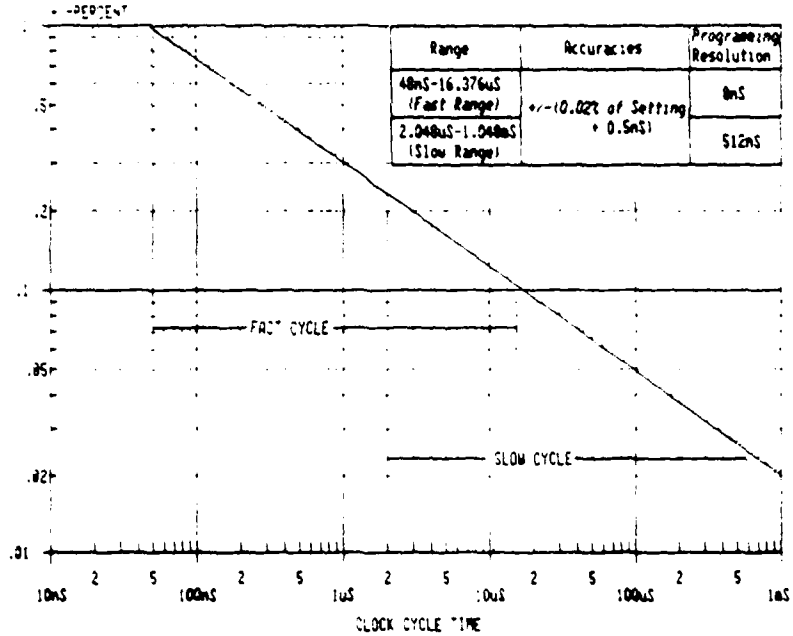


Figure 2-8. S3260/70 - Clock Cycle Accuracies

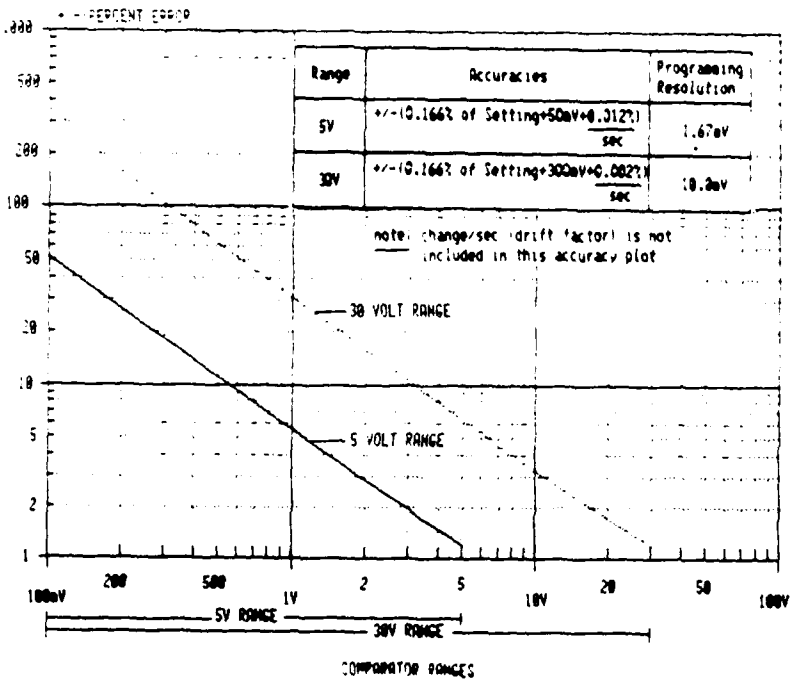


Figure 2-9. S3260/70 - D70 Pin Electronics Card Accuracies

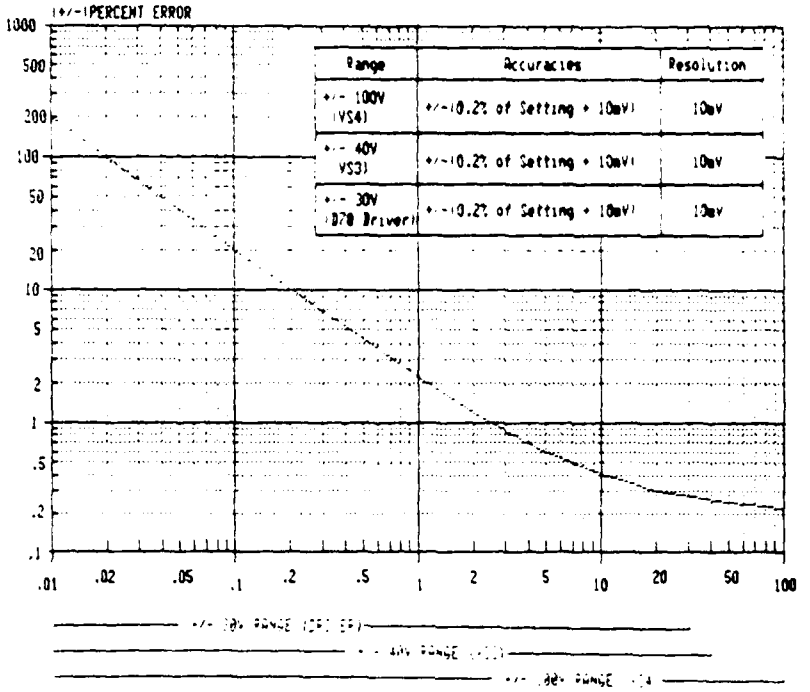


Figure 2-10. S3260/70 - Forcing Voltage Accuracies

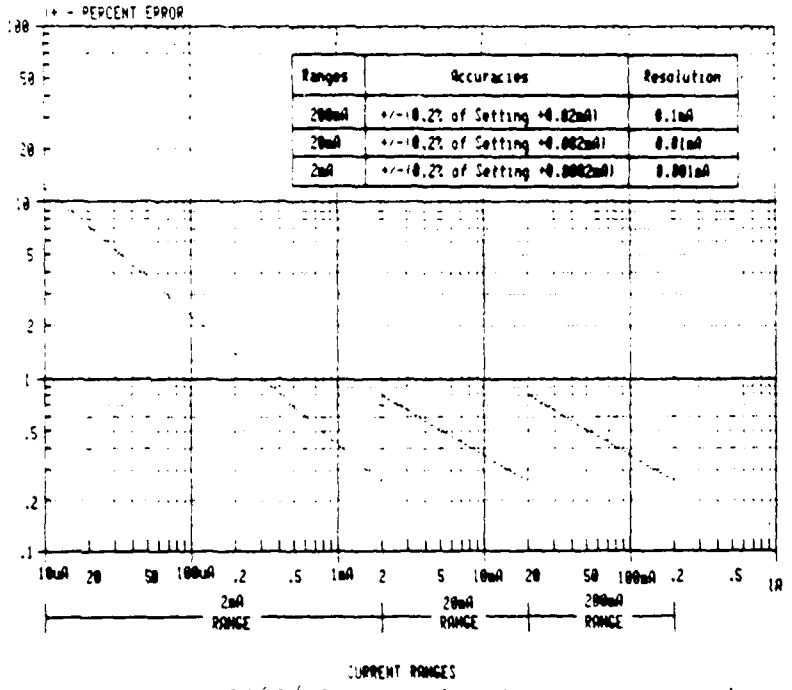


Figure 2-11. S3260/70 - Forcing Current Accuracies

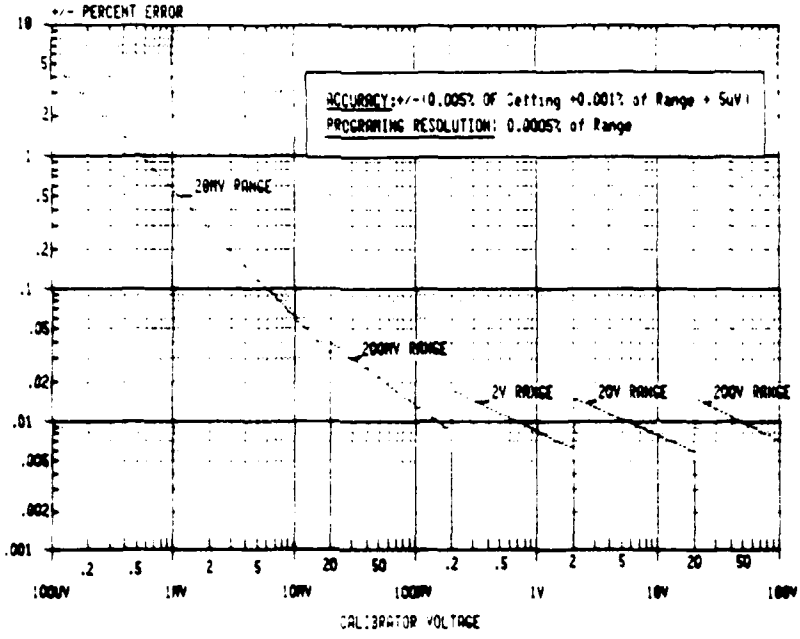


Figure 2-12. Fluke 5100B Meter Calibrator - Forcing Voltage Accuracies

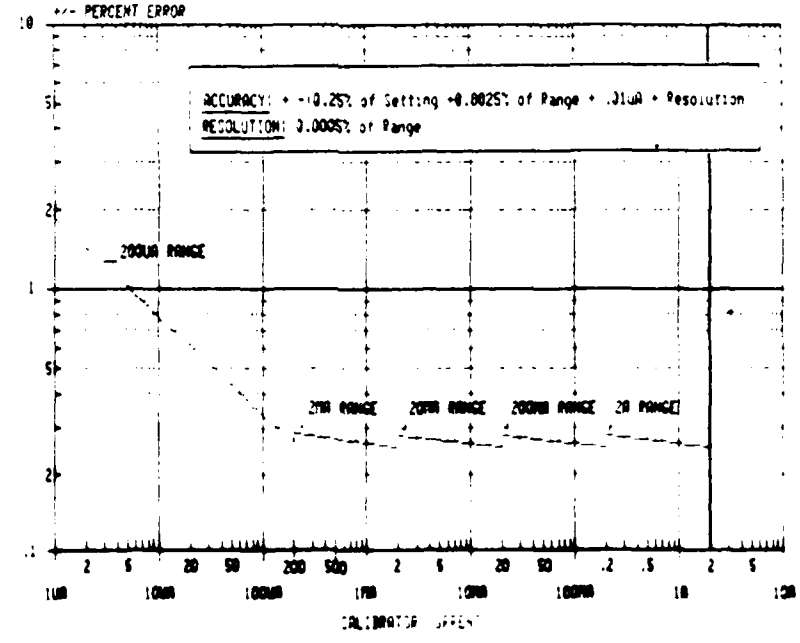


Figure 2-13. Fluke 5100B Meter Calibrator - Forcing Current Accuracies

* = MULTIPLYING D-A CONVERTER DEVICE TYPE 7520 GAIN 4Q 1 LSB= * TYPE										
PARAMETER	-55 TO +125 C			5.0 V			-25 TO +85 C			
	LO-LIM	LIMITS	HI-LIM	LO-LIM	LIMITS	HI-LIM	LO-LIM	LIMITS	HI-LIM	
IR - ALL INPUTS AT 0.0V	0.20	-4.52	100.	0.00	-4.52	100.	0.00	-500.M	100.	UA
IR - ALL INPUTS AT 1.4V	0.20	5.0.	100.	0.00	-4.52	100.	0.00	779.	100.	UA
IR - ALL INPUTS AT 0.8V	0.00	175.M	2.00	0.00	4.52M	2.00	0.00	585.M	2.00	MA
IR - ALL INPUTS AT 2.4V	0.00	2.00	2.00	0.00	1.41	2.00	0.00	585.M	2.00	MA
IREF(+)-ALL INPUTS AT 15V	500.M	1.26	2.00	500.M	1.29	2.00	500.M	1.32	2.00	MA
IREF(-)-ALL INPUTS AT 15V	-2.00	-1.28	-500.M	-2.00	-1.32	-500.M	-2.00	-1.35	-500.M	MA
IIL - ALL INPUTS AT 0.0V	-1.00	PASSED	1.00	-1.00	PASSED	1.00	-1.00	PASSED	1.00	UA
IIL - ALL INPUTS AT 0.8V	-200.	PASSED	1.00	-200.	PASSED	1.00	-200.	PASSED	1.00	UA
IIH - ALL INPUTS AT 15.0V	-1.00	PASSED	1.00	-1.00	PASSED	1.00	-1.00	PASSED	1.00	UA
IIH - ALL INPUTS AT 2.4V	-1.00	PASSED	100.	-1.00	PASSED	100.	-1.00	PASSED	100.	UA
IZS - ALL INPUTS AT 0.0V	-200.	-4.00	200.	-200.	-3.00	200.	-200.	-14.0	200.	NA
IZS - ALL INPUTS AT 2.4V	-200.	-2.00	200.	-200.	-2.50	200.	-200.	-11.0	200.	NA
dIZS/dT - INPUTS AT 0.0V	-50.0	12.5	50.0	0.00	35.0	0.00	-50.0	110.	50.0	PA/oC
dIZS/dT- INPUTS AT 2.4V	-50.0	-6.25	50.0	0.00	60.0	0.00	-50.0	85.0	50.0	PA/oC
GAIN ERROR (VFS)	100.	-34.5	100.	-100.	-29.4	100.	-100.	-22.3	100.	MV
GAIN ERROR (dVFS/dT)	-10.0	6.41	10.0	0.00	-7.30	0.00	-10.0	-7.05	10.0	PPM
PSS - VCC+15V TO 16V	-100.	631.M	100.	-100.	-1.23	100.	-100.	-847.M	100.	PPM
PSS - VCC+15V TO 14V	-100.	-237.M	100.	-100.	385.M	100.	-100.	-1.08	100.	PPM
MSB LINEARITY ERROR - MSB	-500.M	434.M	500.M	-500.M	283.M	500.M	-500.M	285.M	500.M	LSB
BIT LINEARITY ERROR - B2	-500.M	173.M	500.M	-500.M	168.M	500.M	-500.M	173.M	500.M	LSB
BIT LINEARITY ERROR - B3	-500.M	-108.M	500.M	-500.M	-111.M	500.M	-500.M	-117.M	500.M	LSB
BIT LINEARITY ERROR - B4	-500.M	-58.3M	500.M	-500.M	-62.2M	500.M	-500.M	-77.7M	500.M	LSB
BIT LINEARITY ERROR - B5	-500.M	-31.5M	500.M	-500.M	-31.6M	500.M	-500.M	-37.6M	500.M	LSB
BIT LINEARITY ERROR - B6	-500.M	-9.19M	500.M	-500.M	4.52M	500.M	-500.M	17.6M	500.M	LSB
BIT LINEARITY ERROR - B7	-500.M	47.3M	500.M	-500.M	71.6M	500.M	-500.M	94.0M	500.M	LSB
BIT LINEARITY ERROR - B8	-500.M	-37.1M	500.M	-500.M	-23.4M	500.M	-500.M	-12.1M	500.M	LSB
BIT LINEARITY ERROR - B9	-500.M	-26.2M	500.M	-500.M	-15.3M	500.M	-500.M	-6.73M	500.M	LSB
BIT LINEARITY ERROR - LSB	-500.M	-15.6M	500.M	-500.M	-17.2M	500.M	-500.M	-22.0M	500.M	LSB
MAX(+) LINEARITY ERROR &	0.00	389.M	500.M	0.00	437.M	500.M	0.00	473.M	500.M	LSB
ASSOC ADDRESS (ALL CODES)	0.00	776.	0.00	0.00	776.	0.00	0.00	776.	0.00	DEC
MAX(+) LINEARITY ERROR &	0.00	389.M	500.M	0.00	163.M	500.M	0.00	423.M	500.M	LSB
ASSOC ADDRESS (ABBREV)	0.00	776.	0.00	0.00	328.	0.00	0.00	776.	0.00	DEC
MAX(-) LINEARITY ERROR &	-500.M	-368.M	0.00	-500.M	-378.M	0.00	-500.M	-393.M	0.00	LSB
ASSOC ADDRESS (ALL CODES)	0.00	247.	0.00	0.00	247.	0.00	0.00	247.	0.00	DEC
MAX(-) LINEARITY ERROR &	-500.M	-368.M	0.00	-500.M	96.6M	0.00	-500.M	-393.M	0.00	LSB
ASSOC ADDRESS (ABBREV)	0.00	247.	0.00	0.00	931.	0.00	0.00	247.	0.00	DEC
MAX(+) LINEARITY ERROR &	0.00	457.M	500.M	0.00	464.M	500.M	0.00	492.M	500.M	LSB
ASSOC ADDRESS (VREF=+10V)	0.00	776.	0.00	0.00	776.	0.00	0.00	776.	0.00	DEC
MAX(-) LINEARITY ERROR &	-500.M	-360.M	0.00	-500.M	-364.M	0.00	-500.M	-390.M	0.00	LSB
ASSOC ADDRESS (VREF=-10V)	0.00	247.	0.00	0.00	247.	0.00	0.00	247.	0.00	DEC
MAX(+) LINEARITY ERROR &	0.00	444.M	500.M	0.00	427.M	500.M	0.00	532.M	500.M	LSB
ASSOC ADDR (VREF=+1.25V)	0.00	776.	0.00	0.00	776.	0.00	0.00	776.	0.00	DEC
MAX(-) LINEARITY ERROR &	-500.M	-363.M	0.00	-500.M	-397.M	0.00	-500.M	-410.M	0.00	LSB
ASSOC ADDR (VREF=+1.25V)	0.00	247.	0.00	0.00	247.	0.00	0.00	247.	0.00	DEC

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

FIGURE 2-14. Table of Characterization Data for * Converter

55450 DUAL PERIPHERAL POSITIVE-AND DRIVER (STATIC TESTS ONLY)
TEMPERATURE=25DEG C ;DATE=11 DEC 80 TIME=09:36:33

PARAMETER	TEST CONDITIONS		TEST PINS	LO-LIMIT	SN11	SN12	SN13	SN14	SN15	HI-LIMIT	UNITS
VIL	VCC=4.5V		1	800.0M	1.380	1.370	1.370	1.380	1.400	2.000	V
			2	800.0M	1.390	1.380	1.380	1.390	1.410	2.000	V
			13	800.0M	1.390	1.390	1.390	1.390	1.420	2.000	V
VIH	VCC=4.5V		1	800.0M	1.390	1.380	1.380	1.390	1.410	2.000	V
			2	800.0M	1.400	1.390	1.390	1.400	1.420	2.000	V
			13	800.0M	1.400	1.400	1.400	1.400	1.430	2.000	V
VIK	VCC=4.5V	IIC=-12MA	1	-1.500	-985.0M	-990.0M	-1.000	-985.0M	-995.0M	0.000	V
			2	-1.500	-1.150	-1.160	-1.170	-1.155	-1.160	0.000	V
			13	-1.500	-1.155	-1.170	-1.160	-1.165	-1.170	0.000	V
IIH1	VCC=5.5V	VIH=5.5V	1	0.000	26.40U	10.25U	16.20U	14.65U	8.550U	2.000M	A
IIH2	VCC=5.5V	VIH=5.5V	2	0.000	12.10U	5.950U	7.450U	7.850U	4.400U	1.000M	A
			13	0.000	6.250U	4.850U	7.450U	5.500U	3.800U	1.000M	A
IIH1	VCC=5.5V	VIH=2.4V	1	0.000	17.45U	8.050U	12.65U	11.45U	6.900U	20.00U	A
IIH2	VCC=5.5V	VIH=2.4V	2	0.000	7.750U	4.700U	5.800U	6.150U	3.400U	40.00U	A
			13	0.000	5.000U	3.550U	6.950U	5.100U	3.450U	40.00U	A
IIL1	VCC=5.5V	VIL=0.4V	1	-3.200M	-2.100M	-2.145M	-2.155M	-2.145M	-1.990M	0.000	A
IIL2	VCC=5.5V	VIL=0.4V	2	-1.600M	-1.055M	-1.080M	-1.075M	-1.070M	-1.005M	0.000	A
			13	-1.600M	-1.060M	-1.070M	-1.080M	-1.075M	-595.0U	0.000	A
VOL	VCC=4.5V	VIL=0.8V	3	0.000	236.0M	246.5M	259.5M	242.5M	236.5M	500.0M	V
	IOL=16MA		12	0.000	232.0M	242.0M	248.5M	250.5M	236.0M	500.0M	V
VOH	VCC=4.5V	VIH=2.0V	3	2.400	2.695	2.695	2.715	2.725	2.700	4.500	V
	IOH=-400UA		12	2.400	2.725	2.695	2.705	2.730	2.690	4.500	V
IOS1	VCC=4.5V	VIL=0.0V	3	-55.00M	-25.15M	-25.00M	-25.10M	-25.30M	-24.55M	0.000	A
			12	-55.00M	-24.95M	-24.95M	-24.35M	-25.10M	-24.50M	0.000	A
IOS2	VCC=5.5V	VIL=0.0V	3	-55.00M	-32.10M	-31.95M	-32.00M	-32.30M	-31.45M	0.000	A
			12	-55.00M	-31.95M	-31.90M	-31.10M	-32.05M	-31.35M	0.000	A
ICCH	VCC=5.5V	VIH=5.0V	8	0.000	2.275M	2.320M	2.315M	2.315M	2.160M	4.000M	A
ICCL	VCC=5.5V	VIL=0.0V	8	0.000	7.000M	7.100M	7.100M	7.100M	6.600M	11.00M	A

FIGURE 2-5. TABLE OF CHARACTERISTIC DATA FOR PERIPHERAL DRIVERS

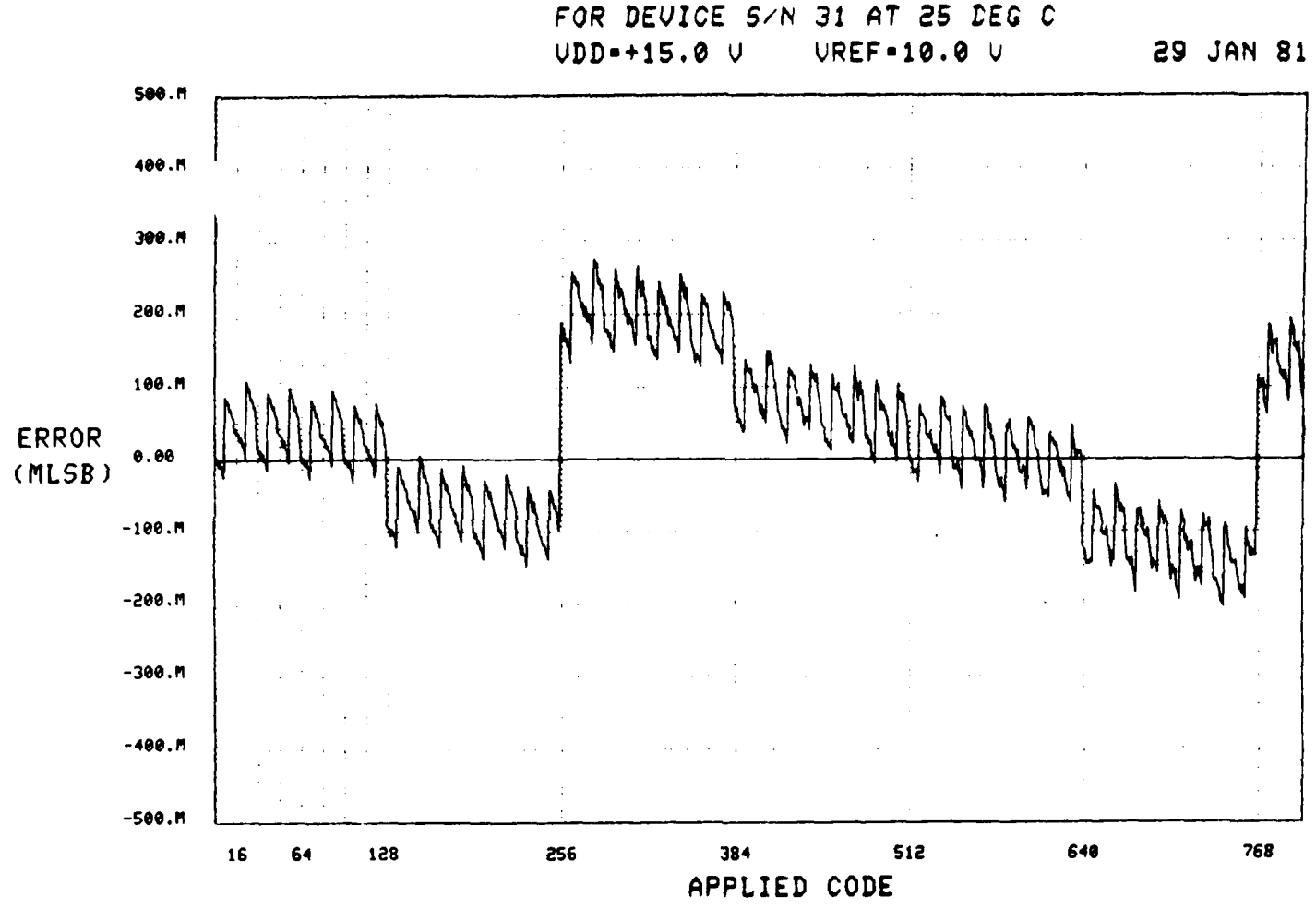


FIGURE 2-16. LINEARITY ERROR (ALL CODES)
7520-10 BIT MULT. D/A CONVERTER

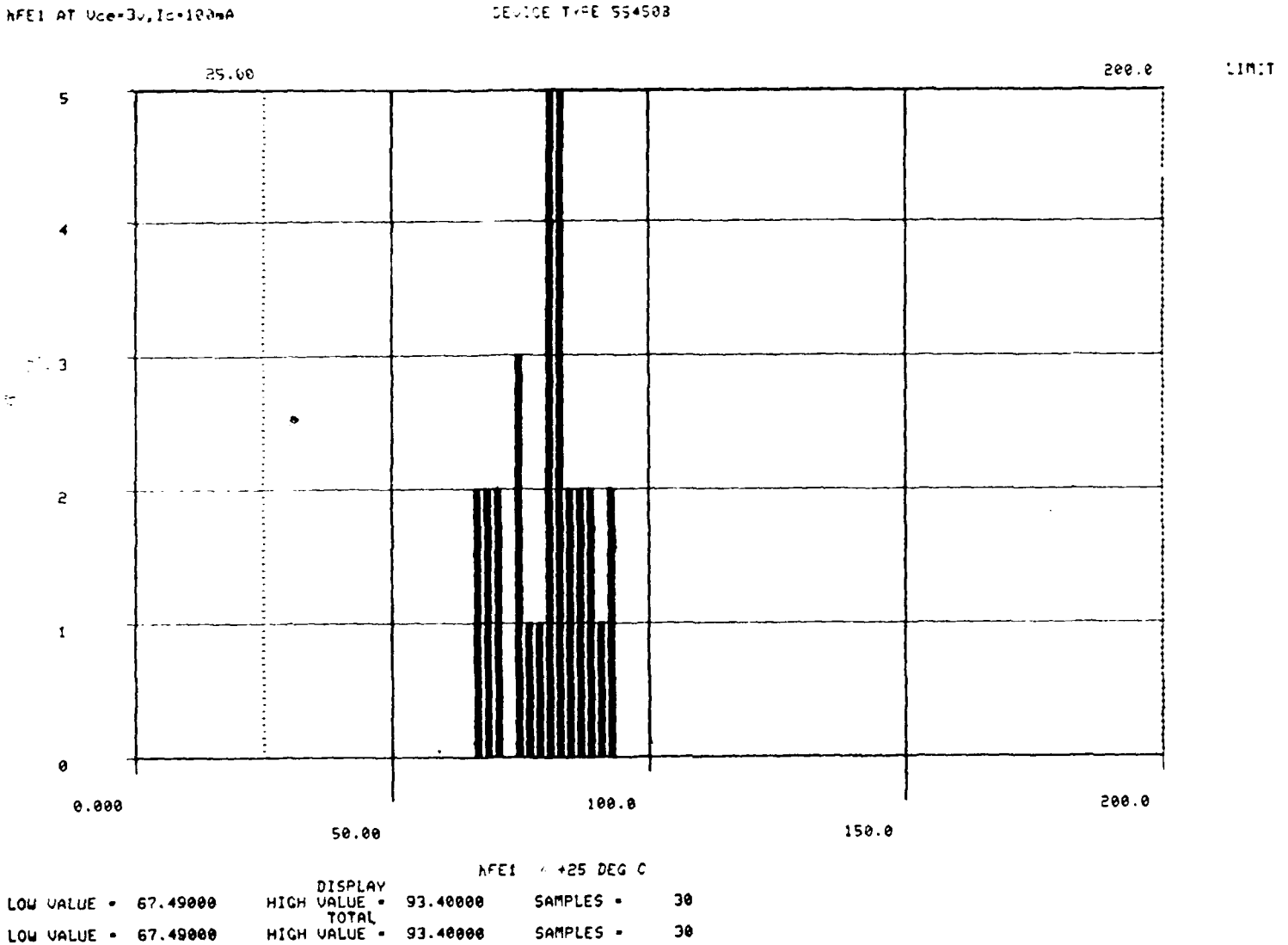


FIGURE 2-17. Histogram Representation of Characterization Data

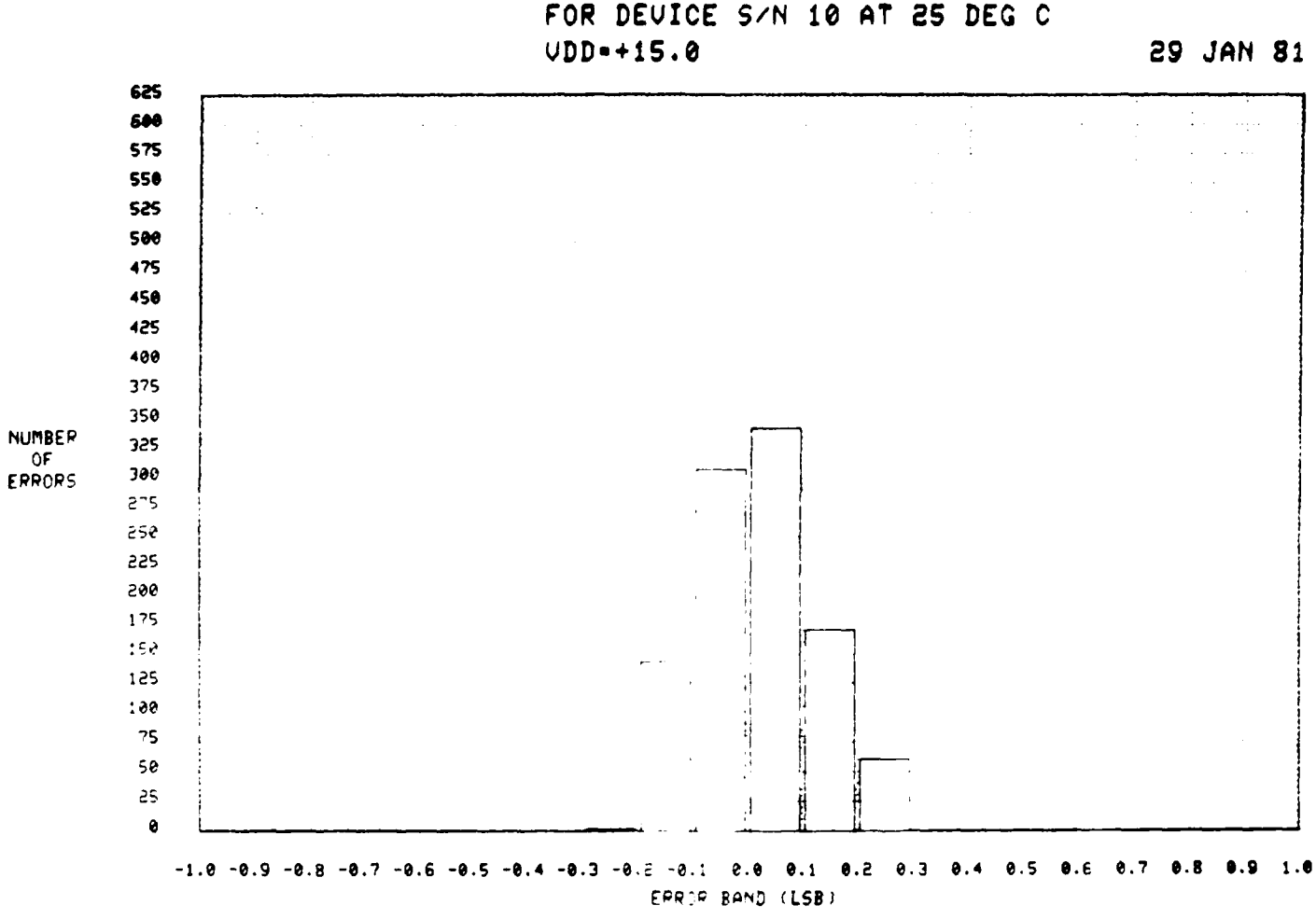


FIGURE 2-1. LINEARITY ERROR DISTRIBUTION
7520-10 BIT CMOS D/A CONVERTER

SECTION III

PERIPHERAL DRIVERS

TABLE OF CONTENTS

Section III

(Characterization of Peripheral Drivers)

3.1 Introduction

Devices for interfacing between TTL logic and the outside world have been a requirement in military systems for as long as TTL logic has been employed in these systems. The devices selected for characterization provide great flexibility in application. The devices can be used as high-speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers. Table 3-1 gives some specifics on the devices tested and their relationship to the military slash sheet device types.

Table 3-1. Table of Device Types Specified.

Military Device Type	Generic Device Type	Manufacturer Symbol	Peripheral Driver Description
12901	55450	N,T	Dual NAND gate and transistor (separate)
12902	55451	N,T	Dual AND, gate and transistor connected
12903	55452	-	Dual NAND gate and transistor connected
12904	55453	N,T	Dual OR, gate and transistor connected
12905	55454	-	Dual NOR, gate and transistor connected
12906	55460	-	High voltage 55450
12907	55461	N,T	High voltage 55451
12908	55462	-	High voltage 55452
12909	55463	N	High voltage 55453
12910	55464	-	High voltage 55454

N = National Semiconductor
T = Texas Instruments

The manufacturer symbol column reflects the source of the devices which were characterized.

[illegible] the features of the 55450/55460 series of devices which helped to [illegible] characterization as a military device types are as follows:

- [illegible]-volt [illegible] output
- [illegible] current (characterized to 300 mA)
- [illegible] switching
- [illegible] positive [illegible]-clamp input
- [illegible] standard [illegible] supply voltages
- [illegible] flexibility in application and [illegible] function

3.2 Description of Device Types

[illegible] diagrams for all of the peripheral drivers are shown in Figure [illegible] and their corresponding schematic circuits are shown in Figure 3-2.

[illegible] of the [illegible] which are [illegible] the [illegible] peripheral drivers with corresponding schematics [illegible] the same references to circuit topology (with the [illegible]/10 series) completes the clamp diodes normally [illegible] the [illegible] to test [illegible]-pole output stages and some minor [illegible] with [illegible] segmental, V_{OH}, V_{IH}, V_{IL}, V_{OH} (TTL [illegible], [illegible], [illegible] (TTL [illegible], [illegible], I_I, I_{IB}, I_{IL}, and I_{OS} [illegible], [illegible] measurements for the peripheral drivers compared [illegible] [illegible] parallel [illegible] gate measurements.

[illegible] the [illegible] peripheral drivers incorporate a high current output stage, [illegible] specification are included for propagation delay measurements, [illegible] [illegible] [illegible], transistor [illegible] saturation voltages, [illegible] [illegible], t_r, t_f, t_{PD}, t_{PLH}, t_{PHL}, V_{OL} and I_{OH}.

[illegible] Test

[illegible] was developed at TRW for the extensive S-3270 test system to [illegible] automatic testing of all peripheral driver devices. All [illegible] functional test recommended by the Joint Committee, including [illegible] functional tests, were incorporated in TEDS as part of the [illegible] [illegible] tests of peripheral drivers was also [illegible] to verify proper [illegible] operation.

[illegible]-3270 Test Adapter

[illegible] adapter, shown in Figure 3-3, was designed to provide the [illegible] interface between the device under test (DUT) and the S-3270

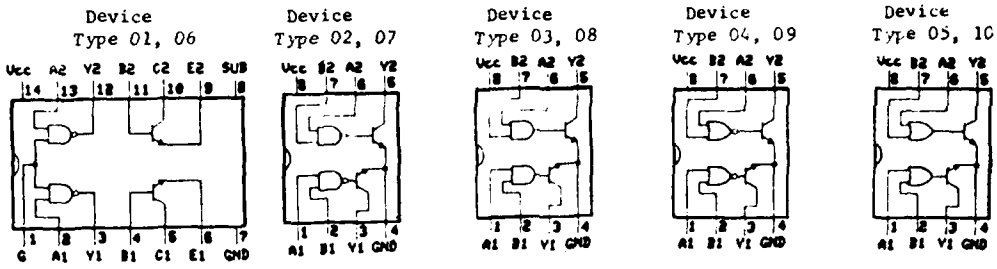


Figure 3-1 Peripheral Driver Block Diagram

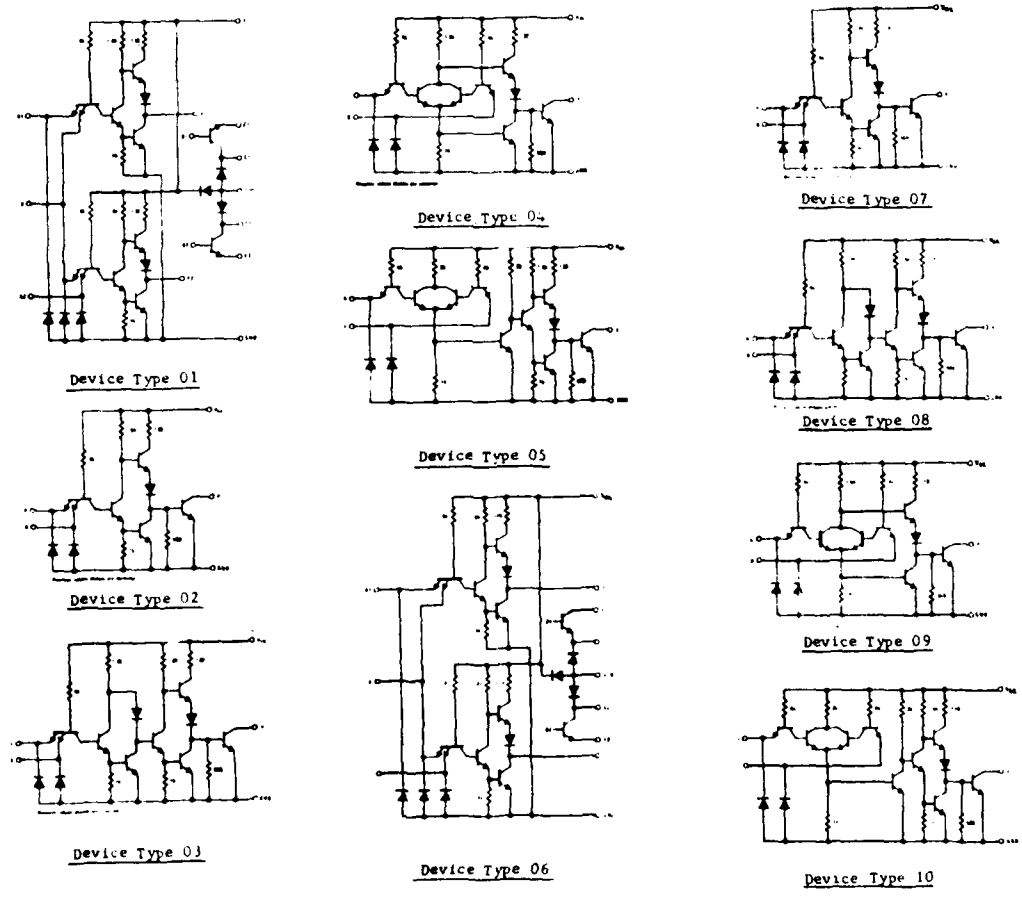


Figure 3-2 Peripheral Driver Schematic Circuits

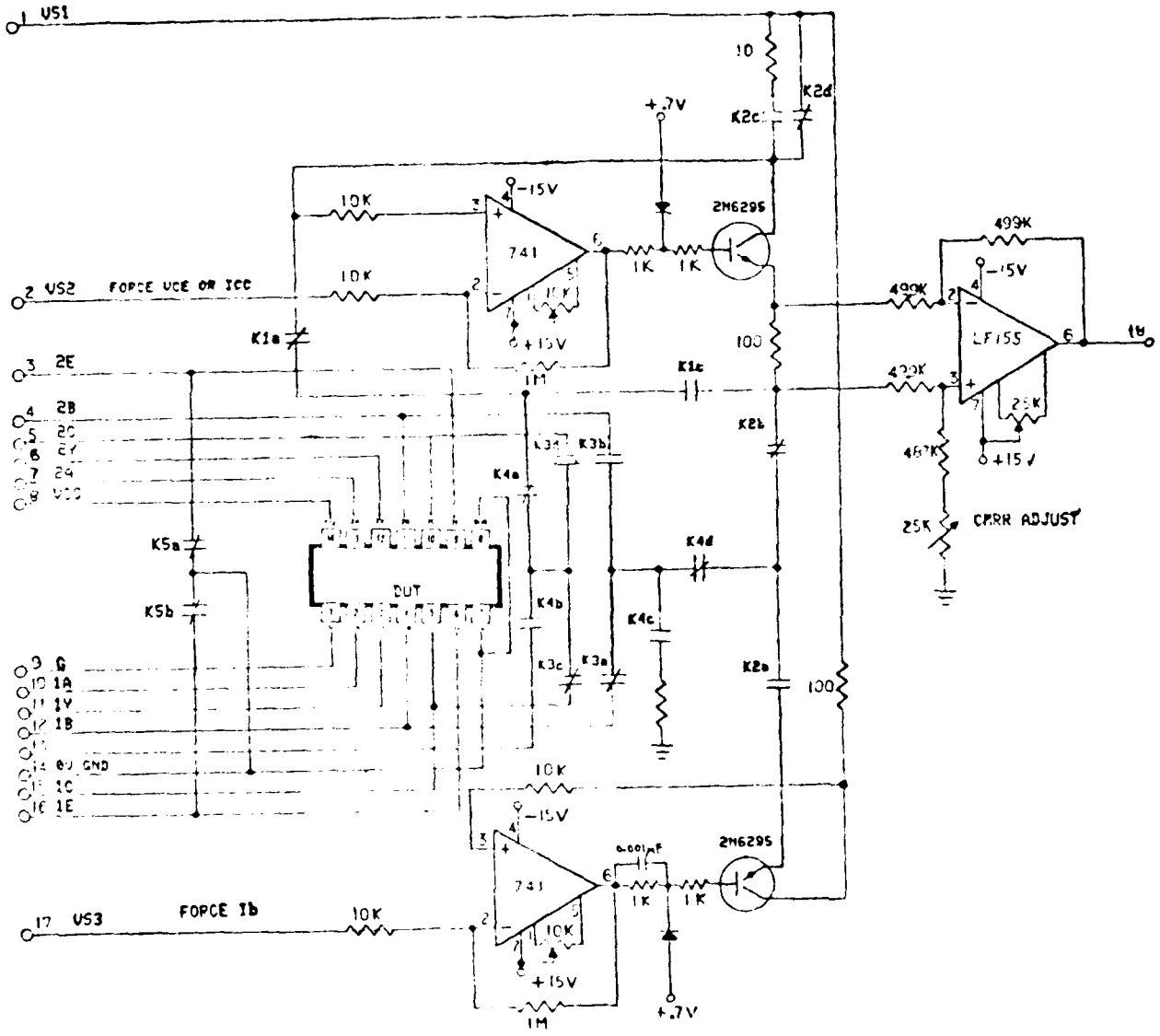


Figure 3-3 Tektronix 1-22 Static Test Adapter

test system. The adapter has the ability to test all static and static pulsed parameters required for characterization of the 55450 and 55460 peripheral drivers.

The adapter consists of Op Amp and transistor circuitry used to force the proper pulsed conditions on the DUT, while stimulated by the S-3270. Actual signal paths to the DUT are implemented by relay control and routed to the S-3270 for testing. All other static tests are performed using the S-3270 driver and measurement system capability.

h_{FE} Tests

Within the "static" test parameters, measurement of h_{FE} was the most difficult. Manufacturers' data sheets specify a t_W = 300 us with a duty cycle $\leq$ 2%. Bench testing indicated that h_{FE} testing could be accurately performed with t_W = 100 us and a duty cycle of 2%. The data sheet specification allows time for the servo circuit used in h_{FE} measurements to reach its final value. A major concern was to minimize the effect of device self heating on parameter measurement.

The Forward Current Transfer Ratio (h_{FE}) of the 55450, 55460 peripheral driver is automated using the circuit shown in Figure 3-4 in conjunction with the S-3270 and the Tektronix Waveform Digitizer option 20 (WFD).

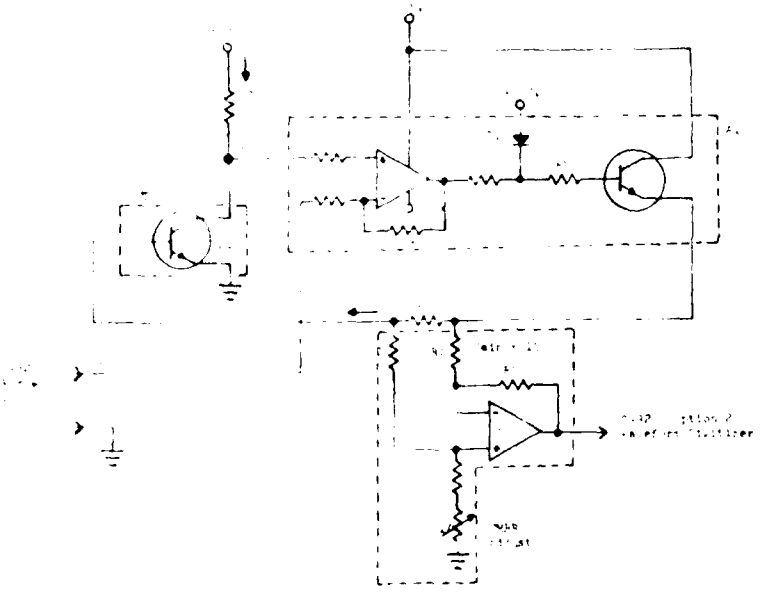


Figure 3-4. h_{FE} Test Circuit.

The criteria for measuring h_{FE} is to force V_{CE} and I_C to predescribed levels while servoing the base current, I_b to achieve these levels. The Forward Current Transfer Ratio h_{FE} becomes

$$h_{FE} = I_C/I_B \text{ with } V_{CE} \text{ constant}$$

The V_{CE} pulse level from the S-3270 is applied to one input of the base drive and comparator amplifier circuit, A1, while the other input to amplifier A1 monitors the V_{CE} level of the DUT. The output of amplifier circuit A1 servos the base current I_B until the DUT's V_{CE} voltage equals the input stimuli from the S-3270. The collector current I_C is forced to the proper level by the relationship of $(V_{CC} - V_C)/R_C$, since V_{CC} and R_C were fixed.

Buffer amplifier A2, senses the voltage drop across resistor R_B, which is proportional to the base current I_B. The buffer amplifier A2 was configured in a differential mode to reduce large common mode voltages present on R_B and to provide increased gain for single-ended measurement capability need by the WFD.

Figure 3-5 illustrates a digitized voltage pulse from across R_B.

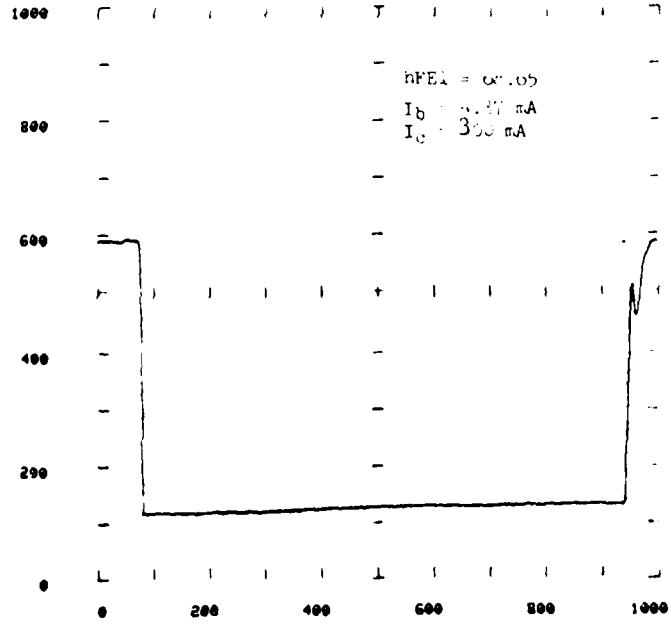


Figure 3-5. h_{FE} measurement waveform.

The voltage translates to 4.370 mA of current. Since the collector current was at 300 mA, h_{FE} is therefore 68.6.

The pulsed measurement techniques were used with V_C of 3 V at currents I_C of 100 mA and 300 mA.

V_{BE} and $V_{CE(SAT)}$

The Base to Emitter Voltage (V_{BE}) and the Collector to Emitter Saturation Voltage ($V_{CE(SAT)}$ pulsed parameters are measured by using the circuit of Figure 3-6 for S-3270 and WFD option 20.

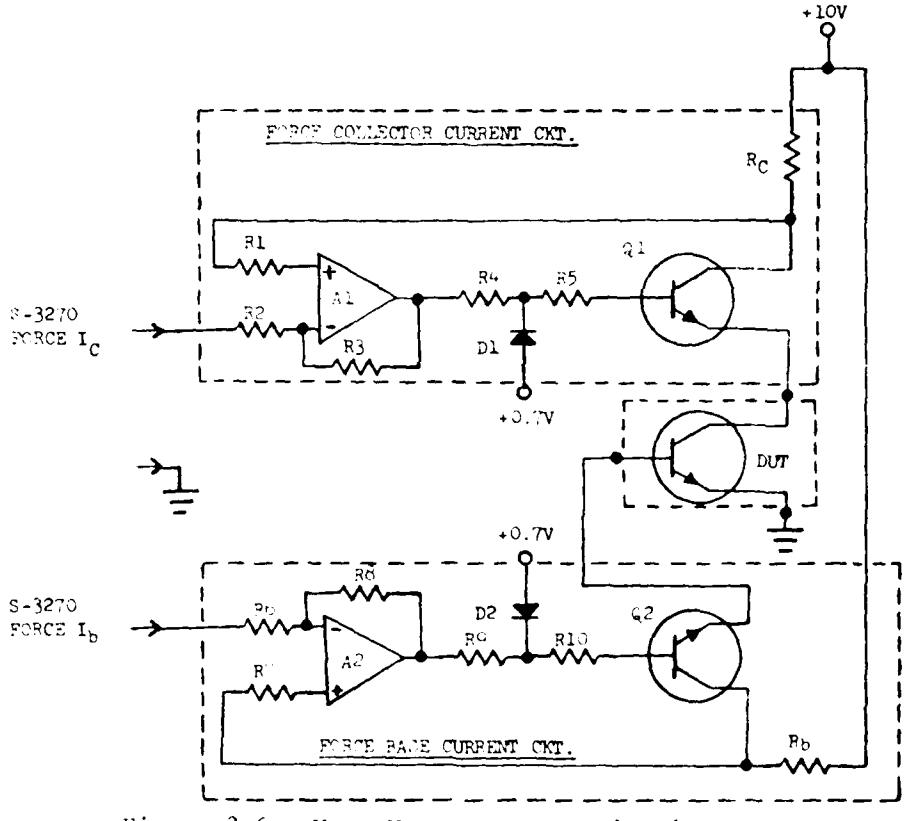


Figure 3-6. V_{BE}, $V_{CE(SAT)}$ test circuit.

The requirements for these tests are to force a given base drive and collector drive current under pulsed conditions, while measuring the resultant base-to-emitter and collector-to-emitter voltages. These

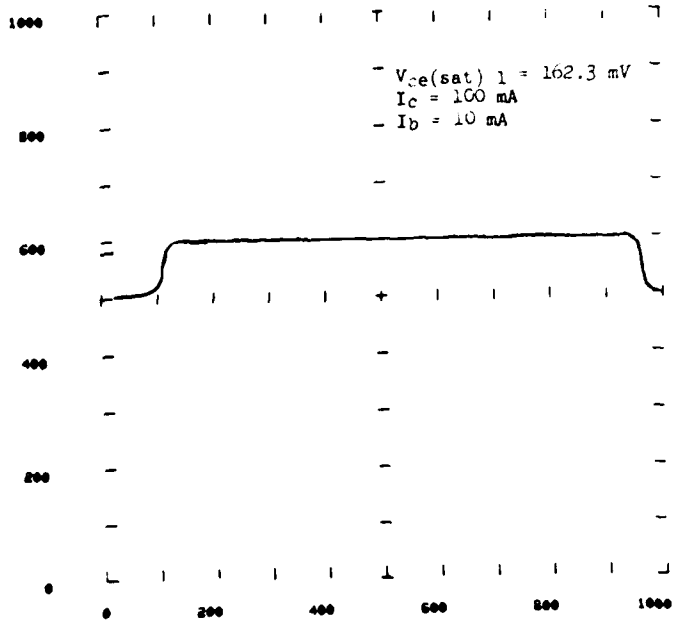


Figure 3-7A $V_{CE(SAT)}$ Measurement Waveform

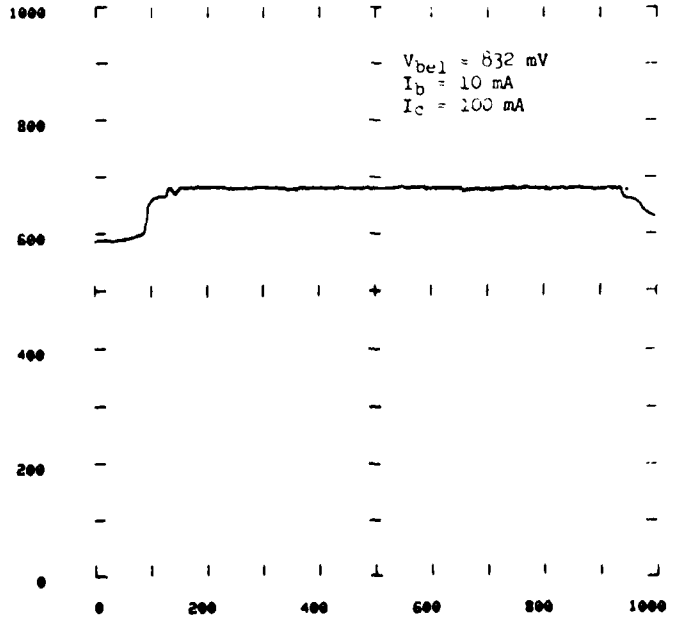


Figure 3-7B V_{BE} Measurement Waveform

are accomplished by applying an S-3270 programmed voltage V_B to one input of comparator amplifier A2. The other input to amplifier A2 monitors the voltage V_B' located a one end of resistor R_B, causing the output of A2 to servo the voltage V_B' until it exactly equals the input stimuli voltage V_B, applied from the S-3270. When these conditions are met, the DUT base current has been forced to the proper drive current level by the relationship of

$$I_B = (V_{BB} - V_B')/R_b$$

since V_{BB} and R_b are constants.

The collector current (I_C) is forced to the proper conditions in much the same way as I_b, with the exception of a much higher current provided by amplifier A1. The relationship of S-3270 input stimuli V_C to forcing current I_C, becomes

$$I_C = (V_{CC} - V_C')_{R_C}$$

Figure 3-7 illustrates digitized waveforms of $V_{CE(SAT)}$ and V_{BE} parameters for a typical 55450 device using a base current I_B = 10 mA and a collector current of 100 mA respectively.

V_{IL} Threshold

Input V_{IL} threshold tests are developed for the S-3270 test system to determine the margin between guaranteed $V_{IL\ max}$ = + 0.8 V and the actual V_{IL} input switching point.

Referring to Figure 3-8, the tests were implemented by pulsing input A, while sampling the output for a change of state.

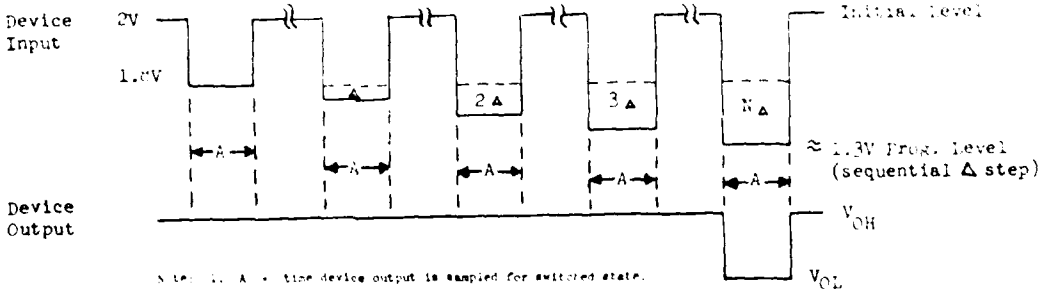
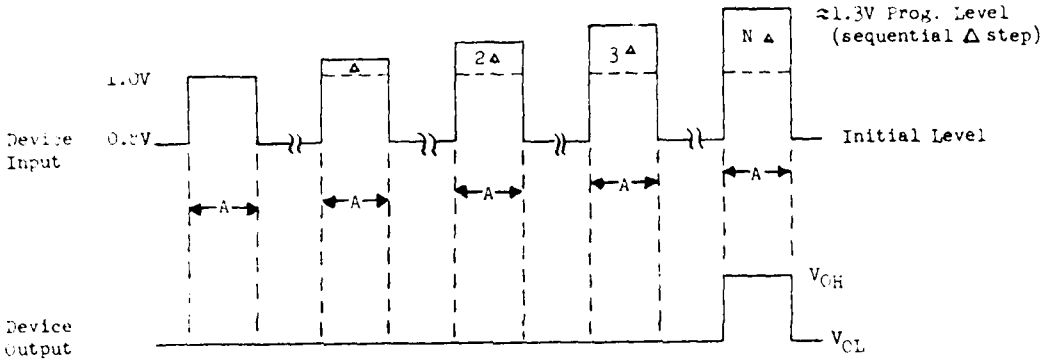


Figure 3-8. V_{IL} Threshold Test.

The initial level starts at + 2.0 V and each succeeding pulse is decremented by -10 mV. During the low level of the pulse, the device output is sampled for the V_{OL} state. If the output fails to switch during the sampling time, the input pulse is returned to + 2.0 V and a new pulse, with a level lowered by - 10 mV is applied to input A. This process is repeated N times, until the output switches to V_{OL}, at which point the V_{IL} value is recorded.

V_{IH} Threshold

The input V_{IH} threshold tests are performed in a similar manner to the V_{IL} threshold tests with the exception of the initial pulse level and the delta increment (refer to Figure 3-9).



Note: 1. A = time device output is sampled for switched state.

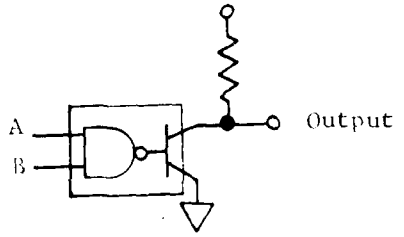


Figure 3-9. V_{IH} Threshold Test.

The initial level starts at + 0.8 V and each succeeding pulse is incremented by + 10 mV. During the high level of the pulse, the device output is sampled for the V_{OH} state. If the output fails to switch to the V_{OH} state during the sampling time, the input pulse is returned to + 0.8 V and a new pulse, with a level increased by + 10 mV.

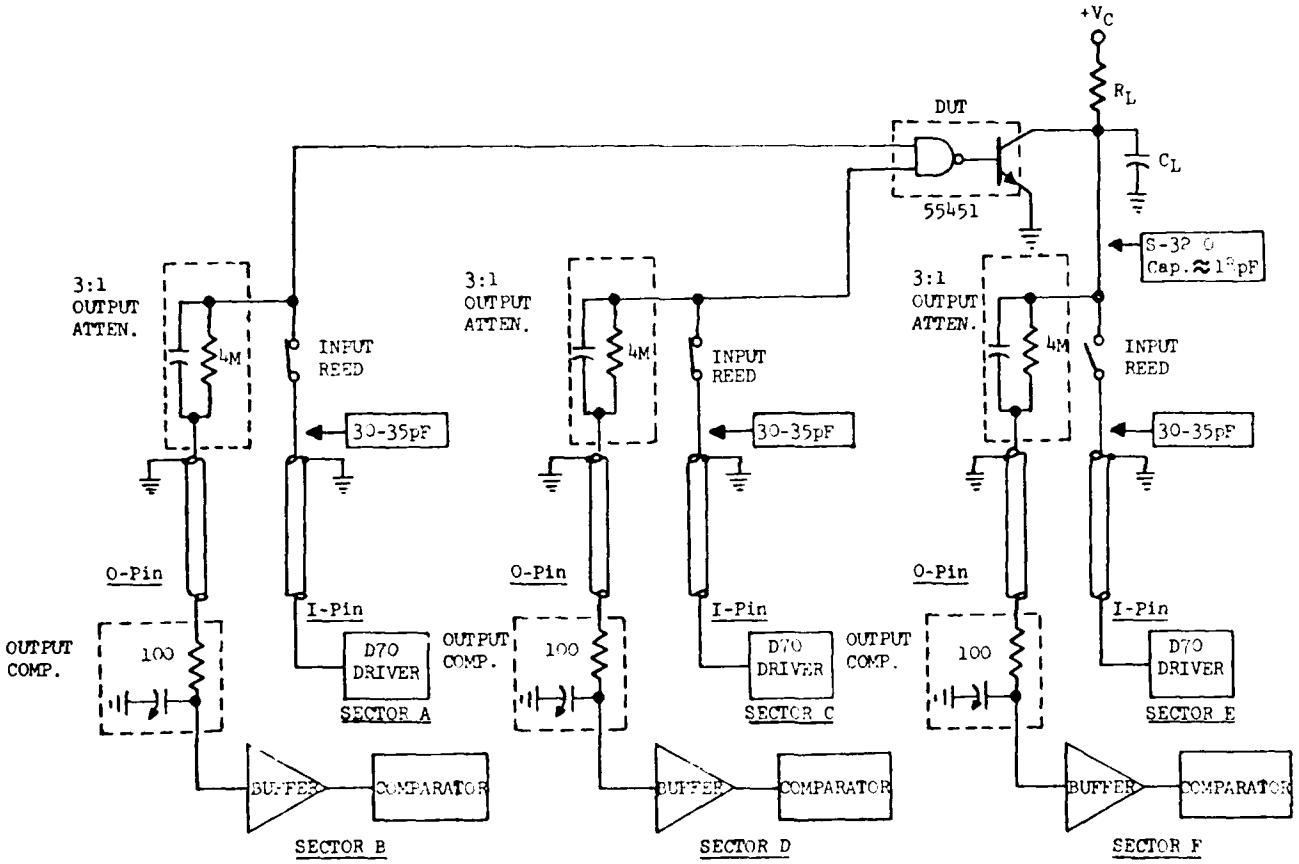


Figure 3-10 Simplified Circuit Diagram of S-3270 Test System with HPO

This process is repeated N times, until the output switches to V_{OH}, at which point the V_{IH} value is recorded.

T_{tLH}, T_{tHL}, T_{PLH}, T_{PHL}

Transition times and propagation delay times for device types (1-10) were measured using the S-3270 test system, the Tektronix High Performance Option (HPO) and a specially constructed test adapter.

The HPO option provides for high accuracy time measurements, skew time corrections, low device pin capacitance ($<$ 18 pF) and buffered scope-type compensation on all device output pins connected to the S-3270 system. A simplified HPO circuit diagram is shown in Figure 3-10, indicating the different signal paths, attenuators, and output compensating networks to provide high accuracy measurements. Correction factors such as skew time between S-3270 sector pins, comparator offsets and output compensator networks are all handled under separate S-3270 calibration procedures to ensure integrity of the system.

Ambiguities can occur as a result of time measurements dependency on supply voltage, temperature, load circuit consideration, layout and test equipment inaccuracies.

Figure 3-11 is the schematic of the load circuit for TTL gates that was proposed by JC-41.

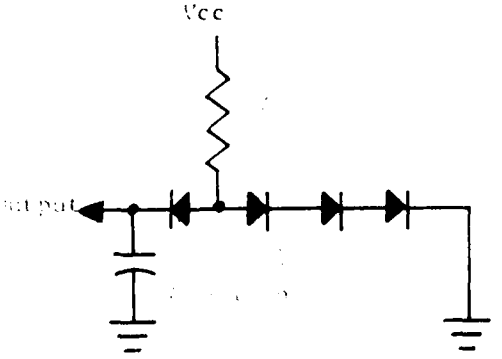


Figure 3-11. JC-41 load circuit for TTL gates.

This circuit is used to simulate 10 standard TTL loads. Comparison of output waveforms obtained with this circuit loading the 55450 "gate" output versus 10 standard TTL gates loading the same gate showed similar results. (See Figure 3-12A, B).

Figure 3-12A

T_{PLH} using JC-41 load circuit
V_{CC} = 4.5 V.

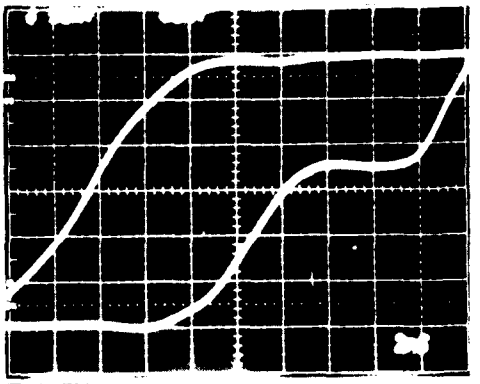
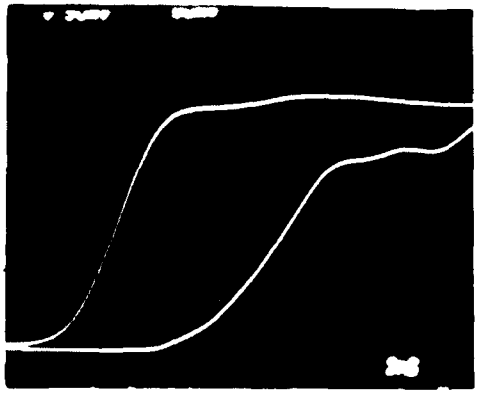


Figure 3-12B

T_{PLH} using 10 TTL gate loading
V_{CC} = 4.5 V



The JC-41 load circuit, however, does not simulate worst case loading. The 400 Ω resistor only gives 10 times the nominal I_{OL} at V_{OL}. No provision was made for simulating I_{OH} loading. C_L isn't high enough to reflect the maximum input capacitances from a TTL gate (approximately 5 pF).

The JC-41 load circuit also increases the ambiguity in propagation delay time measurements.

Propagation delay times are measured at the 1.5 volt points on the input and output waveforms. The flat region in the output waveform occurs near 1.5 V. Propagation delay times can vary by as much as 4 ns as a result of placing the output decision point on the low side or the high side of the flat region in the output waveform. This is clearly unacceptable.

The circuit shown in Figure 3-13 has been used as the load circuit for testing the TTL gate portion of the peripheral driver ICs.

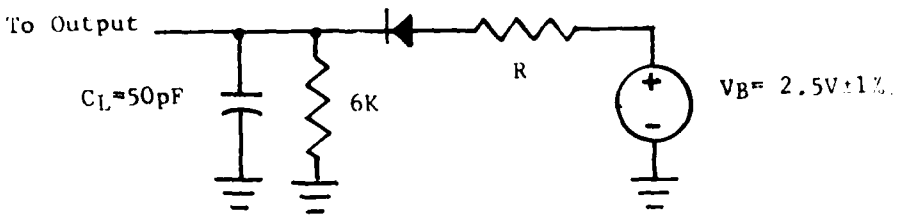


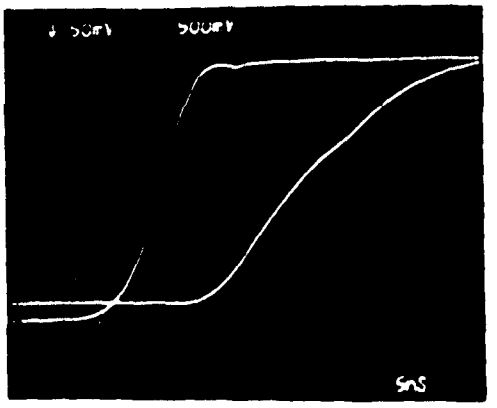
Figure 3-13. Recommended TTL gate load circuit.

This circuit eliminates the ambiguity in propagation delay measurements and also stimulates worst case loading. C_L was raised to give a realistic value for ten TTL gate input capacitances (5 pF/input). R_1 was added to give 10 x I_{IHMAX} . R_2 is selected to give I_O = 10 x I_{ILMAX} at V_{OLMAX}.

Figure 3-14 shows the output waveforms that result after changing the load to the recommended configuration.

Figure 3-14

T_{PLH} using recommended load circuit
V_{CC} = 4.5 V



This additional load capacitance increases T_{PLH}, and the flat region previously noted is eliminated because reverse recovery in D_1 occurs through a higher effective impedance. This eliminates the propagation delay measured ambiguity.

Switching time measurements for the output transistors and for the complete peripheral drivers were also measured with a C_L = 50 pF to reflect a more realistic value of load capacitance.

Supply voltage variations from 4.5 V to 5.5 V have resulted in variations in switching time measurements of up to 2 ns. The majority of devices exhibit slowest switching action at V_{CC} = 4.5 V so this has been selected for these measurements.

Refer to Figure 3-15 for a graph of typical variation in switching parameters with V_{CC}.

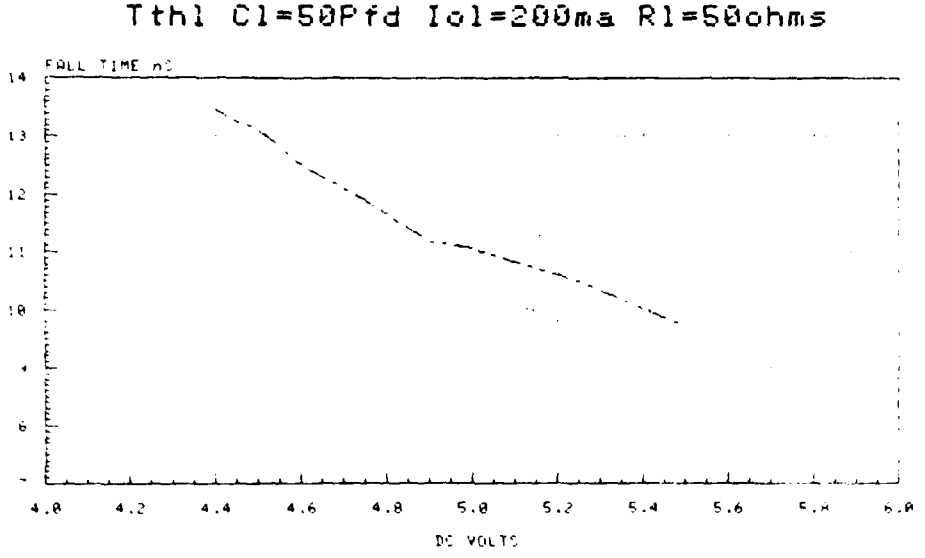


Figure 3-15 T_{HL} vs V_{CC}

Transition time tests were the most difficult to implement, since they involved switching times in the order of 10 ns or less. Careful consideration to the test adapter layout, inductance, capacitance and grounding were critical to ensure that clean output switching waveforms could be achieved.

Figure 3-16 shows typical output transition waveforms from three different vendors.

It should be noted that the output transitions are different in the 80% - 100% and 0% - 20% regions for each vendor.

Correlation of S-3270 transition and propagation time data to bench data was verified by using three independent methods. These verification methods are as follows:

1) Measure data on bench circuit using oscilloscope.
2) Measure S-3270 test adapter on bench using oscilloscope.
3) Measure S-3270 test adapter on S-3270 test system using oscilloscope.

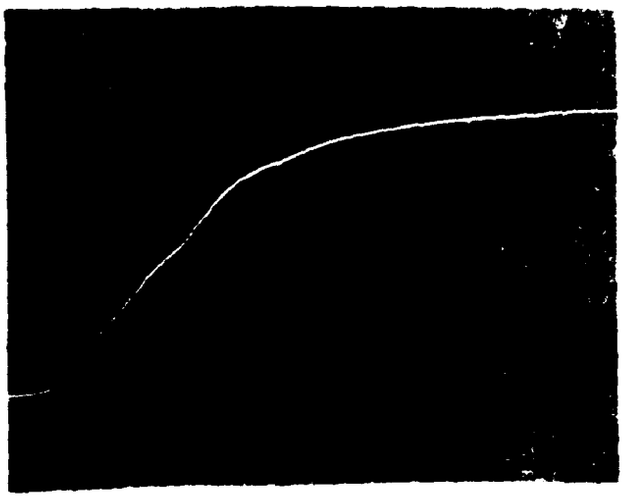


Figure 3-16A

Vendor A

T_{TLH}

Figure 3-16B

Vendor B

T_{TLH}

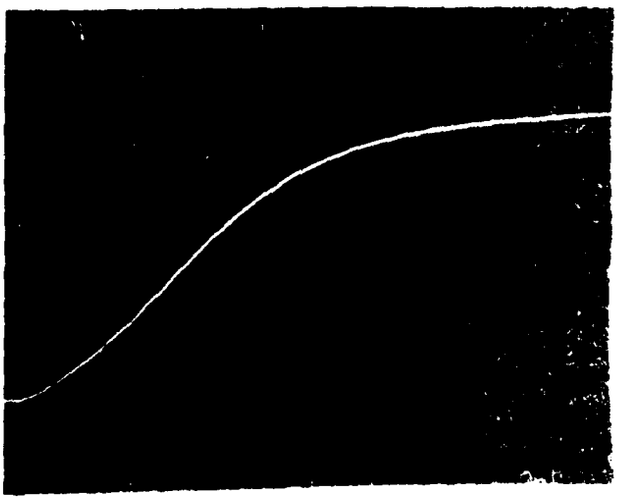


Figure 3-16C

Vendor C

T_{TLH}

3.4 Test Results and Data

A total of 85 peripheral drivers were tested on GEOS' Tektronix S-3270. Each device was sequentially tested at 25°C, -55°C and 125°C.

A typical data sheet for a group of 55450 devices is shown in Table 3-4. Data for up to 5 devices is displayed on a single sheet. This method simplifies comparison of different devices at a single temperatures.

The data was also recorded in the form of histograms for selected parameters at three temperatures. (A sample histogram is given in Table 3-5.) Included were the following:

55460	t_{THL}	t_{PLH}
	t_{TLH}	t_{PHL}
	t_{PHL1}	t_D
	t_{PLH2}	t_R
		t_S
		t_F
	h_{FE} 1,2	V_{CBO1}
	V_{BE} 1,2	V_{CER1}
	V_{CE} 1,2	V_{BEO}
55451	t_{THL}	t_{PLH}
	t_{TLH}	t_{PHL}
55453	t_{THL}	t_{PLH}
	t_{TLH}	t_{PHL}
55461	t_{THL}	t_{PLH}
	t_{TLH}	t_{PHL}
55463	t_{THL}	t_{PLH}
	t_{TLH}	t_{PHL}

This data was published in January 1981 for RADC in a 211 pg handbook entitled:

Characterization Data for MIL-M-38510/129
Peripheral Drivers

(55450, -451, -452, -453, -454
55460, -461, -462, -463, -464)

Sample data sheets and histograms have been included in the Appendix.

3.5 Discussion of Results

Most of the test data taken on the 55450/55460 family of peripheral drivers was within the limits proposed by the JC-41 Committee. The exceptions were the result of changes in test conditions (for example, changing the load circuit for timing tests). Although data on a number of parameters fell within a relatively tight spread relative to the test limits, no attempt was made to tighten the test limits due to the relatively small number of device samples. The exceptions are noted below.

Short-circuit output current (I_{OS})

As originally specified, the I_{OSMIN} specification was tested at V_{CCMAX}. But I_{OSMIN} is lower at V_{CCMIN}. To ensure that I_{OS} would be within the test limits over the full supply voltage range, I_{OSMIN} is tested at V_{CCMIN} and I_{OSMAX} is tested at V_{CCMAX}.

Threshold Voltage (V_T)

Threshold testing of the peripheral drivers gave results that were within the expected range of values. The nominal V_T was approximately 1.3 volts at $T_A = 25°C$ with a d V_T/dT_A approximately -3 mV/°C. This agrees well with measured V_T values for standard TTL.

Breakdown Voltage, V_{CBO}, V_{CER}, V_{EBO}

In all devices tested, V_{CBO} was greater than 17 volts (or nearly 50%) above the minimum breakdown limit. For V_{CER}, all of the devices were greater then 22 volts above the minimum test limit.

Vendor A showed slightly lower V_{EBO} than Vendor B (approximately .5 volts lower on the average).

There were no significant trends observed in breakdown voltages versus temperature.

All breakdown voltages were taken with the substraits pin floating.

Static Forward Current Transfer Ratio (h_{FE})

The JC-41 Committee test conditions specify that h_{FE} is to be measured under pulsed conditions with t_w = 300 us and a duty cycle < 2%. The devices were tested over a range of values for t_w with the duty cycle fixed at 2% with negligible changes in the measured values. T_w was changed to t_w = 100 us to simplify test hardware.

At T_A = 25°, all measured h_{FE}s' exceeded the minimum test limit by greater than two to one. As expected, h_{FE} tended to increase with increasing temperature over the full temperature range. In all cases, the devices tested exceeded the minimum test limit by a reasonable margin.

3.6 Slash Sheet Development

The military specification (MIL-M-38510 slash sheet) on the peripheral drivers was developed in parallel with the characterization effort. The majority of the slash sheet Table I parameters and limits were recommended by the JC-41 Committee on Linear Integrated Circuits. The major changes occurred in the switching time test load circuit and the V_{CC} specification for the switching tests. As a result, the switching parameter test limits were relaxed as needed to accommodate the new test conditions. Also, the I_{OS} testing is now specified at both extremes in supply voltage in order to have the test data reflect the worst case.

3.7 Conclusions and Recommendations

85 generic 55450/460 peripheral drivers were tested on GEOS' S-3270 to characterize their electrical parameters. Bench data was taken to validate S-3270 operation. With the exception of switching time parameters, the devices were well within the test limits.

The switching time of the devices was slowed as a result of the revised test conditions. The test limits for these parameters have been widened to accommodate the test changes.

APPENDIX - SECTION III

PERIPHERAL DRIVERS DATA

SHEETS AND HISTOGRAMS

55450 DUAL PERIPHERAL POSITIVE-AND DRIVER (STATIC TESTS ONLY)
TEMPERATURE=25DEG C ;DATE=09 DEC 80 TIME=11:17:33

PARAMETER	TEST CONDITIONS		TEST PINS	LO-LIMIT	SN1	SN2	SN3	SN4	SN5	HI-LIMIT	UNIT
VIL	VCC=4.5V		1	[illegible]	1.350	1.350	1.350	1.350	1.350	2.000	V
			2	[illegible]	1.340	1.340	1.350	1.350	1.350	2.000	V
			13	800.0M	1.350	1.340	1.330	1.330	1.330	2.000	V
VIH	VCC=4.5V		1	800.0M	1.350	1.330	1.310	1.300	[illegible]	[illegible]	V
			2	800.0M	1.350	1.350	1.340	1.340	[illegible]	[illegible]	V
			13	800.0M	1.350	1.350	1.340	[illegible]	1.350	2.000	V
VIK	VCC=4.5V	IIC=-18MA	1	[illegible]	[illegible]	-910.0M	[illegible]	[illegible]	[illegible]	[illegible]	V
			2	[illegible]	[illegible]	-910.0M	-915.0M	-915.0M	-910.0M	0.000	V
			13	-1.500	970.0M	-920.0M	-925.0M	-925.0M	-920.0M	0.000	V
IIH1	VCC=5.5V	VIH=5.5V	1	0.000	9.650U	8.450U	7.350U	7.250U	9.350U	2.000M	A
IIH2	VCC=5.5V	VIH=5.5V	2	0.000	4.550U	4.[illegible]U	[illegible]	[illegible]	4.400U	[illegible]	A
			13	0.000	4.300U	3.[illegible]U	[illegible]	3.100U	3.700U	[illegible]	A
IIH1	VCC=5.5V	VIH=2.4V	1	0.000	7.350U	6.500U	5.550U	5.550U	7.100U	80.000	A
IIH2	VCC=5.5V	VIH=2.4V	2	0.000	3.650U	3.100U	2.550U	2.550U	3.350U	40.000	A
			13	0.000	3.500U	3.200U	2.800U	2.750U	3.500U	40.000	A
IIL1	VCC=5.5V	VIL=0.4V	1	[illegible]	-2.290M	-2.485M	[illegible]	-2.450M	-2.415M	0.000	A
IIL2	VCC=5.5V	VIL=0.4V	2	[illegible]	1.160M	-1.245M	-1.245M	-1.245M	-1.205M	0.000	A
			13	[illegible]	-1.130M	-1.250M	-1.265M	-1.255M	-1.215M	0.000	A
VOL	VCC=4.5V IOL=16MA	VIL=0.8V	3	0.000	209.5M	171.5M	183.5M	180.0M	178.0M	500.0M	V
			12	0.000	211.0M	172.5M	187.5M	183.5M	175.5M	500.0M	V
VOH	VCC=4.5V IOH=-400UA	VIH=2.0V	3	2.400	2.780	2.760	2.715	2.715	2.765	4.500	V
			12	2.400	2.760	2.760	2.710	2.710	2.760	4.500	V
IOS1	VCC=4.5V	VIL=0.0V	3	-55.00M	[illegible]	[illegible]	[illegible]	[illegible]	-24.50M	0.000	mA
			12	-55.00M	33.80M	-28.65M	-28.40M	-28.00M	-24.75M	0.000	mA
IOS2	VCC=5.5V	VIL=0.0V	3	-55.00M	30.65M	-34.10M	[illegible]	[illegible]	-31.90M	0.000	mA
			12	-55.00M	30.65M	-34.15M	[illegible]	-33.05M	-31.80M	0.000	mA
ICCH	VCC=5.5V	VIH=5.0V	8	0.000	2.405M	[illegible]	[illegible]	[illegible]	2.640M	4.000M	A
ICCL	VCC=5.5V	VIL=0.0V	8	[illegible]	7.600M	8.350M	8.500M	8.350M	[illegible]	11.00M	A

55450 DUAL PERIPHERAL POSITIVE-AND DRIVER (STATIC TESTS ONLY)
TEMPERATURE=25DEG C ;DATE=09 DEC 80 TIME=11:33:29

PARAMETER	TEST CONDITIONS		TEST PINS	LO-LIMIT	SN6	SN7	SN8	SN9	SN10	HI-LIMIT	UNIT
VIL	VCC=4.5V		1 2 13	[illegible] [illegible] [illegible]	1.370 1.340 1.340	1.270 1.320 1.300	1.250 1.280 1.250	1.250 1.310 1.280	1.250 1.250 1.250	2.000 2.000 2.000	V V V
VIH	VCC=4.5V		1 2 13	[illegible] [illegible] 800.0M	1.350 1.360 1.360	1.530 1.330 1.330	1.550 1.330 1.330	1.510 1.330 1.330	1.510 1.310 1.340	2.000 2.000 2.000	V V V
VIK	VCC=4.5V	IIC=-12MA	1 2 13	-1.500 -1.500 -1.500	-915.0M -915.0M -915.0M	-910.0M -910.0M -955.0M	-920.0M -920.0M -950.0M	-915.0M -900.0M -900.0M	-940.0M -885.0M -950.0M	0.000 0.000 0.000	V V V
IIH1	VCC=5.5V	VIH=5.5V	1	0.000	8.050U	10.10U	8.800U	9.500U	8.600U	2.000M	A
IIH2	VCC=5.5V	VIH=5.5V	2 13	0.000 0.000	4.000U 3.200U	5.050U 4.450U	4.300U 3.550U	4.550U 3.800U	4.250U 3.350U	1.000M 1.000M	A A
IIH1	VCC=5.5V	VIH=2.4V	1	0.000	6.100U	7.600U	6.750U	7.200U	6.550U	80.00U	A
II-2	VCC=5.5V	VIH=2.4V	2 13	0.000 0.000	2.950U 3.000U	3.800U 3.600U	3.250U 3.250U	3.550U 3.450U	3.250U 3.050U	40.00U 40.00U	A A
IIL1	VCC=5.5V	VIL=0.4V	1	-3.200M	-2.475M	-2.225M	-2.465M	-2.420M	-2.455M	0.000	A
IIL2	VCC=5.5V	VIL=0.4V	2 13	-1.600M -1.600M	-1.245M -1.245M	-1.120M -1.110M	-1.225M -1.250M	-1.215M -1.215M	-1.235M -1.220M	0.000 0.000	A A
VOL	VCC=4.5V IOL=16MA	VIL=0.8V	3 12	0.000 0.000	179.0M 178.0M	218.0M 216.5M	187.0M 187.0M	186.0M 185.5M	202.0M 202.0M	500.0M 500.0M	V V
VOH	VCC=4.5V IOH=-400UA	VIH=2.0V	3 12	2.400 2.400	2.715 2.730	2.725 2.720	2.725 2.725	2.730 2.725	2.725 2.720	4.500 4.500	V V
IOS1	VCC=4.5V	VIL=0.0V	3 12	-55.00M -55.00M	-25.45M -25.50M	-23.50M -23.00M	-26.10M -26.00M	-26.05M -26.10M	-25.00M -25.65M	0.000 0.000	A A
IOS2	VCC=5.5V	VIL=0.0V	3 12	-55.00M -55.00M	-33.95M -33.55M	-32.85M -32.40M	-33.50M -33.60M	-33.45M -33.50M	-33.15M -32.95M	0.000 0.000	A A
ICCH	VCC=5.5V	VIH=5.0V	8	0.000	2.700M	2.425M	2.705M	2.650M	2.690M	4.000M	A
ICCL	VCC=5.5V	VIL=0.0V	8	0.000	8.250M	7.450M	8.250M	8.150M	8.450M	11.00M	A

55450 DUAL PERIPHERAL POSITIVE-AND DRIVER (STATIC TESTS ONLY)
TEMPERATURE=25DEG C ;DATE=11 DEC 80 TIME=09:36:33

PARAMETER	TEST CONDITIONS		TEST PINS	LO-LIMIT	SN11	SN12	SN13	SN14	SN15	HI-LIMIT	UNITS
VIL	VCC=4.5V		1	[illegible]	1.390	1.370	1.370	1.390	1.400	2.000	V
			2	[illegible]	1.390	1.360	1.380	1.390	1.410	2.000	V
			13	800.0M	1.390	1.390	1.390	1.390	1.420	2.000	V
VIH	VCC=4.5V		1	800.0M	1.300	1.330	1.310	1.300	1.410	2.000	V
			2	800.0M	1.400	1.370	1.370	1.400	1.420	2.000	V
			13	800.0M	1.420	1.400	1.400	1.400	1.430	2.000	V
VIC	VCC=4.5V	IIC=-12MA	1	-1.500	[illegible]	-900.0M	-1.000	-985.0M	-995.0M	0.000	V
			2	-1.500	1.150	-1.160	-1.170	-1.155	-1.160	0.000	V
			13	-1.500	1.155	-1.170	-1.160	-1.165	-1.170	0.000	V
IIH1	VCC=5.5V	VIH=5.5V	1	0.000	26.40U	10.25U	16.20U	14.65U	8.550U	2.000M	A
IIH2	VCC=5.5V	VIH=5.5V	2	0.000	12.10U	5.[illegible]0U	7.450U	7.850U	4.400U	1.000M	A
			13	0.000	6.250U	4.850U	7.400U	5.500U	3.800U	1.000M	A
IIH1	VCC=5.5V	VIH=2.4V	1	0.000	17.45U	8.050U	12.65U	11.45U	6.900U	80.00M	A
IIH2	VCC=5.5V	VIH=2.4V	2	0.000	7.750U	4.[illegible]0U	5.8[illegible]U	6.150U	3.400U	[illegible]	A
			13	0.000	5.000U	3.550U	6.950U	5.100U	3.450U	40.[illegible]	A
IIL1	VCC=5.5V	VIL=0.4V	1	-3.000M	2.100M	-2.145M	-2.155M	-2.145M	-1.990M	0.000	A
IIL2	VCC=5.5V	VIL=0.4V	2	-1.[illegible]M	-1.055M	-1.000M	-1.075M	-1.070M	-1.005M	0.000	A
			13	-1.000M	1.080M	-1.070M	-1.080M	-1.075M	-995.0U	0.000	A
VOL	VCC=4.5V	VIL=0.8V	3	0.000	236.0M	246.5M	259.5M	242.5M	236.5M	500.0M	V
	IOL=16MA		12	0.000	232.0M	242.0M	248.5M	230.5M	236.0M	500.0M	V
VOH	VCC=4.5V	VIH=2.0V	3	2.400	2.605	2.605	2.715	2.765	2.700	4.500	V
	IOH=-400UA		12	2.400	2.705	2.695	2.705	2.730	2.690	4.500	V
IOS1	VCC=4.5V	VIL=0.0V	3	-55.00M	-25.10M	-[illegible].00M	-25.10M	-[illegible].30M	-24.55M	0.000	A
			12	-55.00M	-24.85M	-24.95M	-24.85M	-25.10M	-24.50M	0.000	A
IOS2	VCC=5.5V	VIL=0.0V	3	-50.[illegible]	-32.10M	-31.[illegible]M	-32.[illegible]M	-32.00M	-31.45M	0.000	A
			12	-50.[illegible]	-31.[illegible]M	-31.[illegible]1	-31.10M	-32.05M	-31.35M	0.000	A
ICCH	VCC=5.5V	VIH=5.0V	8	0.000	2.[illegible]75M	2.[illegible]0M	2.315M	2.315M	2.160M	4.000M	A
ICCL	VCC=5.5V	VIL=0.2V	8	0.000	7.[illegible]0M	7.100M	7.100M	7.100M	6.[illegible]0M	11.[illegible]M	A

SG460 DUAL PERIPHERAL POSITIVE-AND DRIVER (STATIC TESTS ONLY)
TEMPERATURE=25DEG C ;DATE=09 DEC 80 TIME=09:38:37

PARAMETER	TEST CONDITIONS		TEST PIN#	LO-LIMIT	SN1	SN2	SN3	SN4	SN5	HI-LIMIT	UNITS
VCE1	IC=100UA	IE=0	5 10	35.00 35.00	53.55 53.75	53.60 81.45	72.70 73.60	66.80 75.15	69.75 73.15	100.0 100.0	V V
VCER	IC=100UA	Rbe=500	5 10	30.00 30.00	55.60 53.55	52.35 81.60	73.80 73.40	64.55 75.20	67.90 73.55	100.0 100.0	V V
VEB0	IE=100UA	IC=0	5 10	5.000 5.000	6.010 5.995	6.350 6.350	6.235 6.220	6.235 6.240	6.235 6.235	25.00 25.00	V V
HFE1	Vce=3V	IC=100MA	5 10	35.00 35.00	73.30 80.93	83.17 90.19	80.93 82.62	84.39 80.24	75.50 76.23	200.0 200.0	# #
HFE2	Vce=3V	IC=300MA	5 10	30.00 30.00	73.99 75.17	73.76 77.13	74.46 75.89	77.38 78.15	68.82 69.02	200.0 200.0	# #
VBE1	Ib=10MA	IC=100MA	4 11	0.000 0.000	742.2M 805.6M	805.6M 831.0M	805.6M 818.3M	805.6M 831.0M	805.6M 831.0M	1.000 1.000	V V
VBE2	Ib=30MA	IC=300MA	4 11	0.000 0.000	889.1M 854.5M	957.9M 945.2M	932.5M 930.2M	945.2M 945.2M	945.2M 945.2M	1.200 1.200	V V
VCEST1	Ib=10MA	IC=100MA	5 10	0.000 0.000	277.9M 227.1M	303.2M 290.6M	265.2M 268.6M	265.2M 265.2M	290.6M 277.9M	400.0M 400.0M	V V
VCEST2	Ib=30MA	IC=300MA	5 10	0.000 0.000	377.4M 275.9M	415.5M 402.8M	352.5M 357.0M	352.0M 352.0M	377.9M 377.4M	700.0M 700.0M	V V

55450 DUAL PERIPHERAL POSITIVE-AND DRIVER (STATIC TESTS ONLY)
TEMPERATURE=25DEG C ;DATE=10 DEC 80 TIME=10:06:53

PARAMETER	TEST CONDITIONS		TEST PIN#	LO-LIMIT	SN6	SN7	SN8	SN9	SN10	HI-LIMIT	UNITS
VCEO	IC=100UA	IE=0	5 10	35.00 35.00	72.75 81.95	71.50 71.15	69.75 70.00	70.45 70.60	74.80 74.75	100.0 100.0	V V
VCER	IC=100UA	Rbe=500	5 10	30.00 30.00	72.40 81.75	71.20 71.55	70.00 70.00	70.35 70.30	74.00 74.45	100.0 100.0	V V
VEBO	IE=100UA	IC=0	5 10	5.000 5.000	6.320 6.320	6.230 6.230	6.250 6.250	6.265 6.255	6.360 6.360	25.00 25.00	V V
HFE1	Vce=3V	IC=100MA	5 10	25.00 25.00	82.02 85.31	81.77 83.50	67.71 68.90	70.75 71.40	92.30 93.40	200.0 200.0	* *
HFE2	Vce=3V	IC=300MA	5 10	30.00 30.00	73.53 74.70	75.17 76.14	63.13 62.46	65.58 67.07	84.58 85.19	200.0 200.0	* *
VBE1	Ib=10MA	IC=100MA	4 11	0.600 0.600	805.6M 818.3M	818.3M 818.3M	818.3M 831.0M	818.3M 818.3M	818.3M 818.3M	1.000 1.000	V V
VBE2	Ib=30MA	IC=300MA	4 11	0.600 0.600	957.9M 952.8M	932.5M 945.2M	957.9M 946.5M	945.2M 932.5M	932.5M 931.6M	1.200 1.200	V V
VCESAT1	Ib=10MA	IC=100MA	5 10	0.000 0.000	277.9M 290.6M	277.8M 285.6M	290.6M 265.8M	285.2M 265.3M	252.4M 252.5M	400.0M 400.0M	V V
VCESAT2	Ib=30MA	IC=300MA	5 10	0.000 0.000	390.1M 408.6M	386.7M 389.3M	377.4M 389.3M	339.3M 339.0M	326.7M 326.3M	700.0M 700.0M	V V

SG150 DUAL PERIPHERAL POSITIVE-AND DRIVER (STATIC TESTS ONLY)
TEMPERATURE=25DEG C ;DATE=10 DEC 80 TIME=16:03:22

PARAMETER	TEST CONDITIONS		TEST PIN#	LO-LIMIT	SN11	SN12	SN13	SN14	SN15	HI-LIMIT	UNITS
VCEO	IC=100UA	IE=0	5 10	35.00 35.00	52.85 53.15	59.55 59.75	60.65 62.30	61.35 61.60	58.55 58.60	100.0 100.0	V V
VCER	IC=100UA	Rbe=500	5 10	30.00 30.00	52.90 53.25	59.55 59.85	60.70 62.40	61.40 61.65	58.60 58.70	100.0 100.0	V V
VECO	IE=100UA	IC=0	5 10	5.000 5.000	6.780 6.785	6.835 6.825	6.785 6.680	6.820 6.835	6.960 6.960	25.00 25.00	V V
HFE1	Vce=3V	IC=100MA	5 10	25.00 25.00	63.25 67.49	81.62 82.62	75.67 74.19	87.62 89.71	80.39 82.74	200.0 200.0	# #
HFE2	Vce=3V	IC=300MA	5 10	30.00 30.00	62.97 61.89	73.53 74.02	68.28 67.46	73.67 75.71	75.64 77.15	200.0 200.0	# #
VBE1	Ib=10MA	IC=100MA	4 11	0.000 0.000	817.6M 826.8M	805.2M 815.4M	805.6M 817.8M	804.4M 818.3M	808.7M 831.0M	1.000 1.000	V V
VBE2	Ib=30MA	IC=300MA	4 11	0.000 0.000	935.5M 942.0M	934.5M 945.0M	947.8M 947.6M	945.2M 945.8M	932.5M 932.5M	1.200 1.200	V V
VCEST1	Ib=10MA	IC=100MA	5 10	0.000 0.000	269.6M 269.2M	265.2M 267.8M	287.6M 289.2M	265.2M 266.0M	265.2M 264.8M	400.0M 400.0M	V V
VCEST2	Ib=30MA	IC=300MA	5 10	0.000 0.000	349.6M 351.2M	349.5M 351.8M	350.5M 351.2M	353.6M 353.8M	325.5M 324.8M	700.0M 700.0M	V V

55450 DUAL PERIPHERAL POSITIVE-AND DRIVER (GATES & TRANSISTORS COMBINED)
TEMPERATURE=25DEG C ;DATE=08 DEC 80 TIME=17:22:56

PARAMETER	TEST CONDITIONS		TEST PINS	LO-LIMIT	SN1	SN2	SN3	SN4	SN5	HI-LIMIT	UNITS
TPHL	VCC=4.5V IOL=200MA	CL=50PFD RL=50	5 10	0.000 0.000	9.308N 9.258N	10.66N 10.66N	9.208N 9.258N	9.208N 9.308N	9.358N 9.658N	15.00N 15.00N	S S
TTLH	VCC=4.5V IOL=200MA	CL=50PFD RL=50	5 10	0.000 0.000	9.128N 8.428N	9.170N 8.760N	8.970N 8.378N	9.020N 8.420N	8.920N 8.420N	12.00N 12.00N	S S
TPLH	VCC=4.5V IOL=200MA	CL=50PFD RL=50	1 2 13	0.000 0.000 0.000	15.70N 15.64N 15.24N	15.76N 15.71N 15.31N	15.49N 15.43N 15.03N	15.92N 15.87N 15.47N	15.22N 15.17N 14.77N	30.00N 30.00N 30.00N	S S S
TPHL	VCC=4.5V IOL=200MA	CL=50PFD RL=50	1 2 13	0.000 0.000 0.000	18.32N 18.11N 17.76N	18.90N 18.76N 18.41N	18.12N 17.92N 17.57N	18.27N 18.07N 17.72N	18.06N 17.88N 17.53N	30.00N 30.00N 30.00N	S S S

55450 DUAL PERIPHERAL POSITIVE-AND DRIVER (GATES & TRANSISTORS COMBINED)
TEMPERATURE=25DEG C ;DATE=08 DEC 80 TIME=17:17:17

PARAMETER	TEST CONDITIONS		TEST PINS	LO-LIMIT	SN6	SN7	SN8	SN9	SN10	HI-LIMIT	UNITS
TPHL	VCC=4.5V IOL=200MA	CL=50PFD RL=50	5 10	0.000 0.000	10.62N 10.62N	9.108N 9.208N	9.408N 9.558N	9.308N 9.508N	9.308N 9.408N	15.00N 15.00N	S S
TTLH	VCC=4.5V IOL=200MA	CL=50PFD RL=50	5 10	0.000 0.000	9.072N 8.372N	9.070N 8.270N	8.870N 8.320N	8.870N 8.320N	9.070N 8.320N	12.00N 12.00N	S S
TPLH	VCC=4.5V IOL=200MA	CL=50PFD RL=50	1 2 13	0.000 0.000 0.000	16.00N 15.94N 15.54N	15.46N 15.41N 15.01N	14.72N 14.66N 14.26N	14.94N 14.89N 14.49N	15.21N 15.74N 15.34N	30.00N 30.00N 30.00N	S S S
TPHL	VCC=4.5V IOL=200MA	CL=50PFD RL=50	1 2 13	0.000 0.000 0.000	18.72N 18.51N 18.16N	18.17N 17.97N 17.62N	17.92N 17.72N 17.37N	17.87N 17.67N 17.32N	18.62N 18.59N 18.24N	30.00N 30.00N 30.00N	S S S

55450 DUAL PERIPHERAL POSITIVE-AND DRIVER (GATES & TRANSISTORS COMBINED)
TEMPERATURE=25DEG C ;DATE=08 DEC 80 TIME=17:30:25

PARAMETER	TEST CONDITIONS		TEST PINS	LO-LIMIT	SN11	SN12	SN13	SN14	SN15	HI-LIMIT	UNITS
TTHL	VCC=4.5V IOL=200MA	CL=50PFD RL=50	5 10	0.000 0.000	11.16N 11.61N	10.26N 10.25N	10.11N 10.41N	9.608N 9.708N	10.46N 10.71N	15.00N 15.00N	S S
TTLH	VCC=4.5V IOL=200MA	CL=50PFD RL=50	5 10	0.000 0.000	10.47N 9.470N	10.17N 9.370N	10.02N 9.720N	10.42N 9.470N	9.970N 9.170N	12.00N 12.00N	S S
TPLH	VCC=4.5V IOL=200MA	CL=50PFD RL=50	1 2 13	0.000 0.000 0.000	21.47N 21.61N 20.96N	19.09N 18.60N 18.20N	18.83N 18.15N 17.75N	19.53N 19.45N 19.05N	19.73N 19.68N 19.28N	30.00N 30.00N 30.00N	S S S
TPHL	VCC=4.5V IOL=200MA	CL=50PFD RL=50	1 2 13	0.000 0.000 0.000	22.55N 22.42N 22.07N	19.54N 19.40N 19.05N	18.84N 18.67N 18.32N	18.56N 18.40N 18.05N	20.67N 20.56N 20.21N	30.00N 30.00N 30.00N	S S S

55450 DUAL PERIPHERAL POSITIVE-AND DRIVER (SWITCHING TIME-TTL GATE ONLY)
TEMPERATURE=25DEG C ;DATE=15 DEC 80 TIME=15:52:02

PARAMETER	TEST CONDITIONS		TEST PINS	LO-LIMIT	SN1	SN2	SN3	SN4	SN5	HI-LIMIT	UNITS
TPLH1	VCC=4.5V CL=50PFD	IOL=16MA	1 2 13	0.000 0.000 0.000	11.50N 12.15N 10.93N	12.02N 12.61N 11.35N	10.87N 11.46N 10.24N	12.44N 13.03N 11.81N	12.21N 12.80N 11.59N	22.00N 22.00N 22.00N	S S S
TPHL2	VCC=4.5V CL=50PFD	IOL=16MA	1 2 13	0.000 0.000 0.000	7.04[illegible]N 7.[illegible]N 6.[illegible]N	8.[illegible]N 8.10[illegible]N 7.19[illegible]N	7.4[illegible]N 7.[illegible]N 6.48[illegible]N	8.4[illegible]N 8.[illegible]N 7.516N	8.[illegible]N 8.[illegible]N 7.3[illegible]N	30.00N 30.00N 30.00N	S S S

55450 DUAL PERIPHERAL POSITIVE-AND DRIVER (SWITCHING TIME-TTL GATE ONLY)
TEMPERATURE=25DEG C ;DATE=15 DEC 80 TIME=16:11:51

PARAMETER	TEST CONDITIONS		TEST PINS	LO-LIMIT	SN6	SN7	SN8	SN9	SN10	HI-LIMIT	UNITS
TPLH1	VCC=4.5V CL=50PFD	IOL=16MA	1 2 13	0.000 0.000 0.000	11.44N 12.09N 10.87N	12.01N 12.66N 11.43N	10.85N 11.50N 10.27N	11.01N 11.66N 10.43N	10.08N 11.52N 10.35N	22.00N 22.00N 22.00N	S S S
TPHL2	VCC=4.5V CL=50PFD	IOL=16MA	1 2 13	0.000 0.000 0.000	7.0[illegible]N 7.[illegible]N 6.830N	8.[illegible]N 8.[illegible]N 7.638N	8.077N 8.[illegible]N 7.714N	7.[illegible]N 7.[illegible]N 6.514N	7.4[illegible]N 7.421N 6.541N	30.00N 30.00N 30.00N	S S S

55450 DUAL PERIPHERAL POSITIVE-AND DRIVER (SWITCHING TIME-TTL GATE ONLY)
TEMPERATURE=25DEG C ;DATE=15 DEC 80 TIME=16:25:31

PARAMETER	TEST CONDITIONS		TEST PINS	LO-LIMIT	SN11	SN12	SN13	SN14	SN15	HI-LIMIT	UNITS
TPLH1	VCC=4.5V CL=50PFD	IOL=16MA	1 2 13	0.000 0.000 0.000	14.[illegible]N 14.[illegible]N 12.[illegible]N	13.[illegible]N 14.[illegible]N 12.40N	13.15N 14.01N 12.[illegible]N	14.37N 14.[illegible]N 13.[illegible]N	13.22N 13.81N 11.93N	22.00N 22.00N 22.00N	S S S
TPHL2	VCC=4.5V CL=50PFD	IOL=16MA	1 2 13	0.000 0.000 0.000	11.[illegible]N 11.[illegible]N 10.14N	12.[illegible]N 12.[illegible]N 9.[illegible]N	10.[illegible]N 10.[illegible]N 9.488N	11.[illegible]N 11.34N 10.21N	10.58N 10.[illegible]N 9.[illegible]N	30.00N 30.00N 30.00N	S S S

55450 DUAL PERIPHERAL POSITIVE-AND DRIVER (SWITCHING TIME-TRANSISTOR ONLY)
TEMPERATURE=25DEG C ;DATE=15 DEC 80 TIME=19:46:41

PARAMETER	TEST CONDITIONS		TEST PINS	LO-LIMIT	SN1	SN2	SN3	SN4	SN5	HI-LIMIT	UNITS
TD	IB=20MA CI=50PFD	IC=200MA RI=50	1 2	0.000 0.000	8.340N 8.120N	8.920N 8.470N	8.420N 8.520N	9.110N 8.970N	8.570N 8.050N	15.00N 15.00N	S S
TP	IB=20MA CI=50PFD	IC=200MA RI=50	1 2	0.000 0.000	8.760N 8.570N	8.670N 8.620N	8.760N 8.400N	9.180N 9.230N	8.540N 8.700N	20.00N 20.00N	S S
TS	IB=20MA CI=50PFD	IC=200MA RI=50	1 2	0.000 0.000	11.30N 11.05N	11.99N 11.33N	11.39N 11.27N	12.17N 12.01N	11.44N 11.25N	15.00N 15.00N	S S
TF	IB=20MA CI=50PFD	IC=200MA RI=50	1 2	0.000 0.000	9.010N 8.940N	8.670N 8.670N	8.970N 8.770N	9.030N 9.030N	8.750N 8.670N	15.00N 15.00N	S S

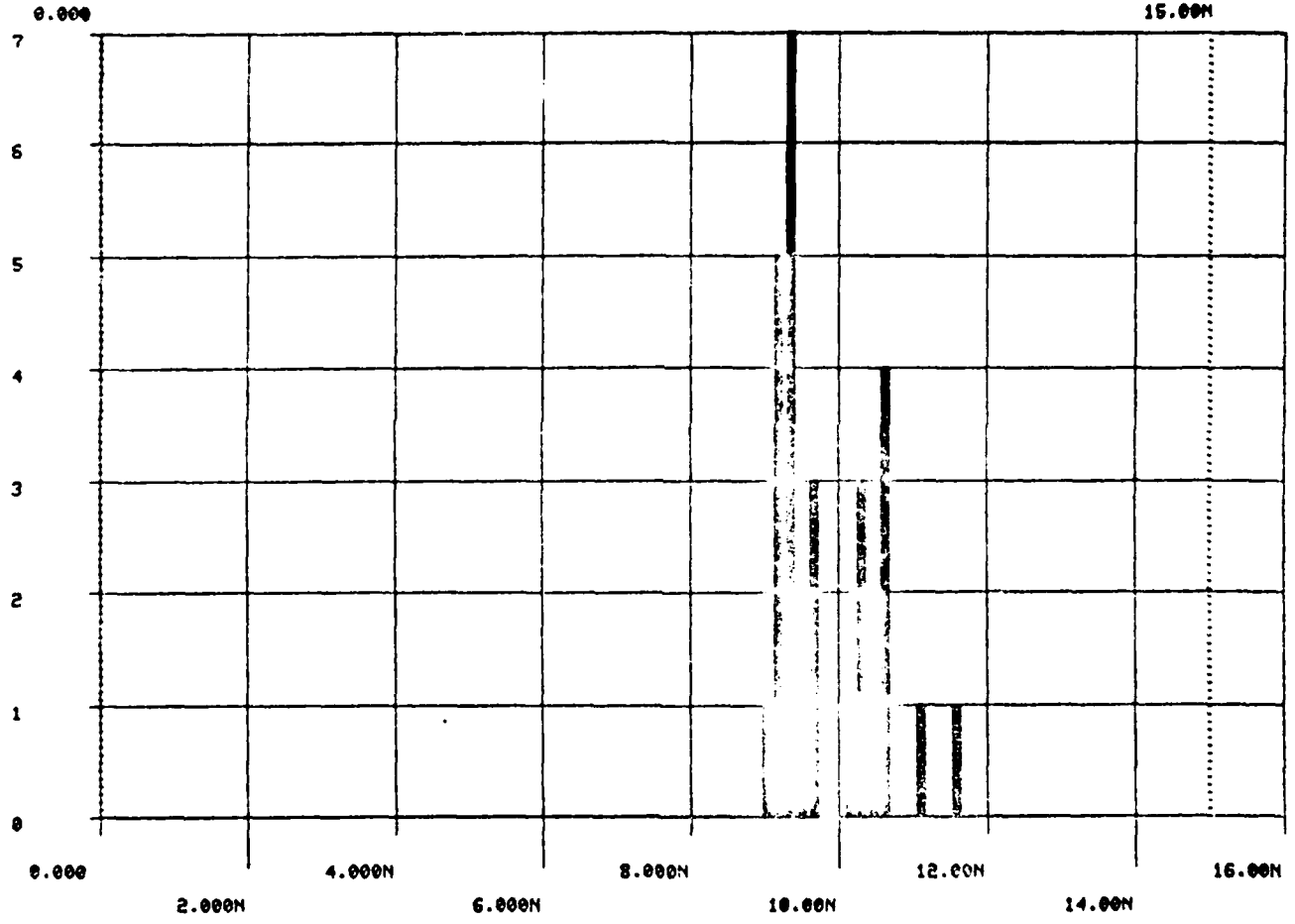
55450 DUAL PERIPHERAL POSITIVE-AND DRIVER (SWITCHING TIME-TRANSISTOR ONLY)
TEMPERATURE=25DEG C ;DATE=15 DEC 80 TIME=19:10:56

PARAMETER	TEST CONDITIONS		TEST PINS	LO-LIMIT	SN6	SN7	SN8	SN9	SN10	HI-LIMIT	UNITS
TD	IB=20MA CI=50PFD	IC=200MA RI=50	1 2	0.000 0.000	9.140N 9.020N	8.930N 8.820N	8.970N 8.630N	8.530N 8.470N	9.150N 8.930N	15.00N 15.00N	S S
TP	IB=20MA CI=50PFD	IC=200MA RI=50	1 2	0.000 0.000	9.280N 9.040N	8.650N 8.400N	9.000N 8.870N	8.980N 8.740N	9.170N 9.110N	20.00N 20.00N	S S
TS	IB=20MA CI=50PFD	IC=200MA RI=50	1 2	0.000 0.000	11.37N 11.03N	11.80N 11.31N	11.40N 11.02N	11.47N 11.22N	11.14N 10.97N	15.00N 15.00N	S S
TF	IB=20MA CI=50PFD	IC=200MA RI=50	1 2	0.000 0.000	10.10N 9.070N	9.110N 8.910N	9.410N 9.220N	9.400N 9.370N	9.310N 9.300N	15.00N 15.00N	S S

55450 DUAL PERIPHERAL POSITIVE-AND DRIVER (SWITCHING TIME-TRANSISTOR ONLY)
TEMPERATURE=25DEG C ;DATE=15 DEC 80 TIME=19:30:47

PARAMETER	TEST CONDITIONS		TEST PINS	LO-LIMIT	SN11	SN12	SN13	SN14	SN15	HI-LIMIT	UNITS
TD	IB=20MA CL=50PFD	IC=200MA RL=50	1 2	0.000 0.000	8.700N 8.610N	9.870N 9.000N	10.77N 10.78N	8.550N 8.410N	9.720N 9.000N	15.00N 15.00N	S S
TR	IB=20MA CL=50PFD	IC=200MA RL=50	1 2	0.000 0.000	9.700N 9.600N	10.41N 10.32N	10.13N 9.940N	9.210N 9.070N	10.78N 10.53N	20.00N 20.00N	S S
TS	IB=20MA CL=50PFD	IC=200MA RL=50	1 2	0.000 0.000	11.77N 11.61N	11.31N 11.07N	11.62N 11.08N	11.87N 11.78N	11.13N 11.13N	15.00N 15.00N	S S
TF	IB=20MA CL=50PFD	IC=200MA RL=50	1 2	0.000 0.000	9.600N 9.570N	10.37N 10.12N	9.700N 9.650N	10.10N 10.03N	10.51N 10.35N	15.00N 15.00N	S S

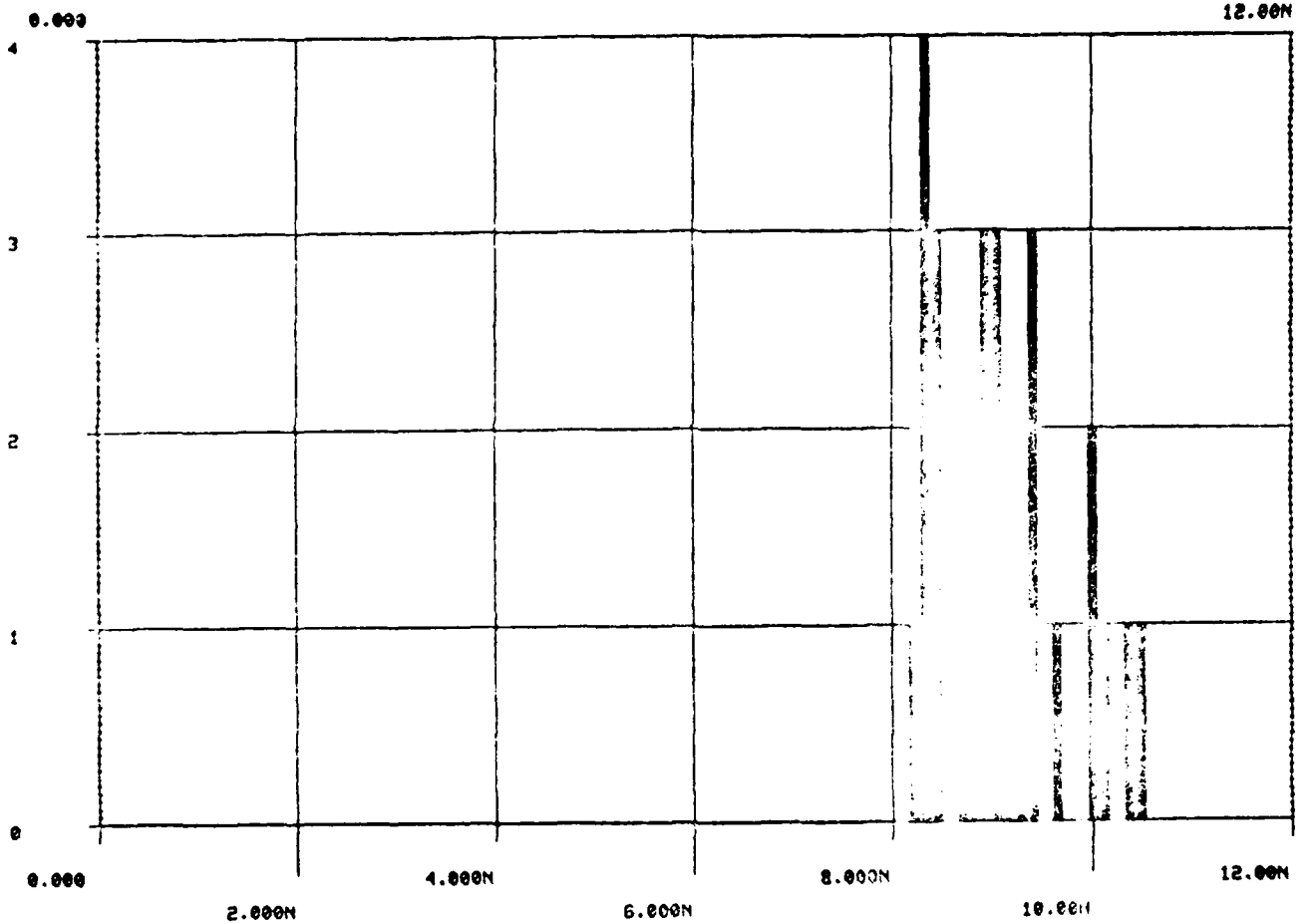
VALUE AT 5 FROM D04S0.LOG:JED 08:19:59 17 DEC 89
TTHL AT VCC-4.5V DEVICE TYPE 54S03



TTHL @ +25 DEG C

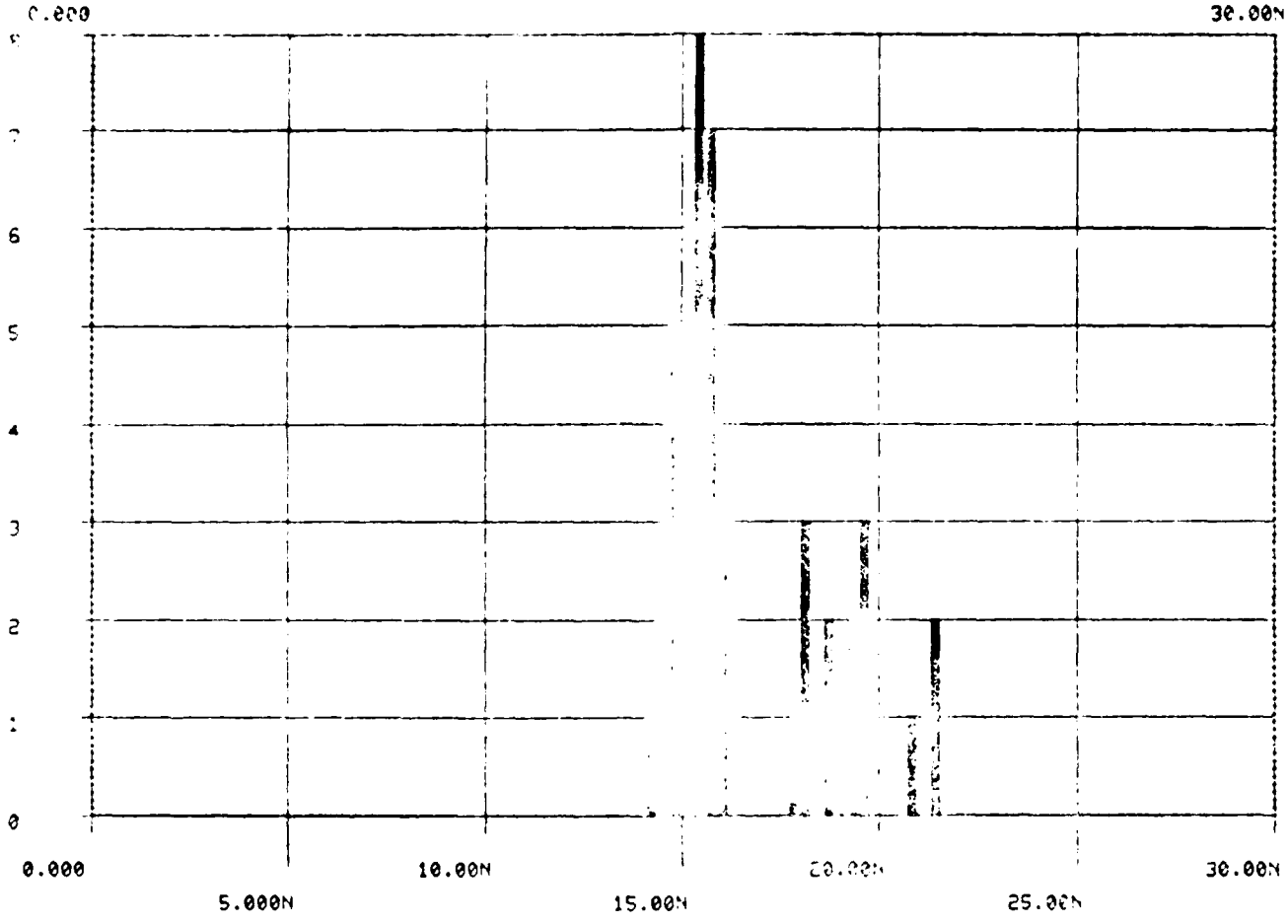
	DISPLAY				
LOW VALUE =	9.103000N	HIGH VALUE =	11.60300N	SAMPLES =	30
	TOTAL				
LOW VALUE =	9.103000N	HIGH VALUE =	11.60300N	SAMPLES =	30

VALUE AT 5 FROM D1430.LOG:JED 08:26:58 17 DEC 80
TTLH AT VCC=4.5V DEVICE TYPE 54S08



TTLH @ +25 DEG C

LOW VALUE =	8.269999N	DISPLAY HIGH VALUE =	10.47000N	SAMPLES =	30
LOW VALUE =	8.269999N	TOTAL HIGH VALUE =	10.47000N	SAMPLES =	30



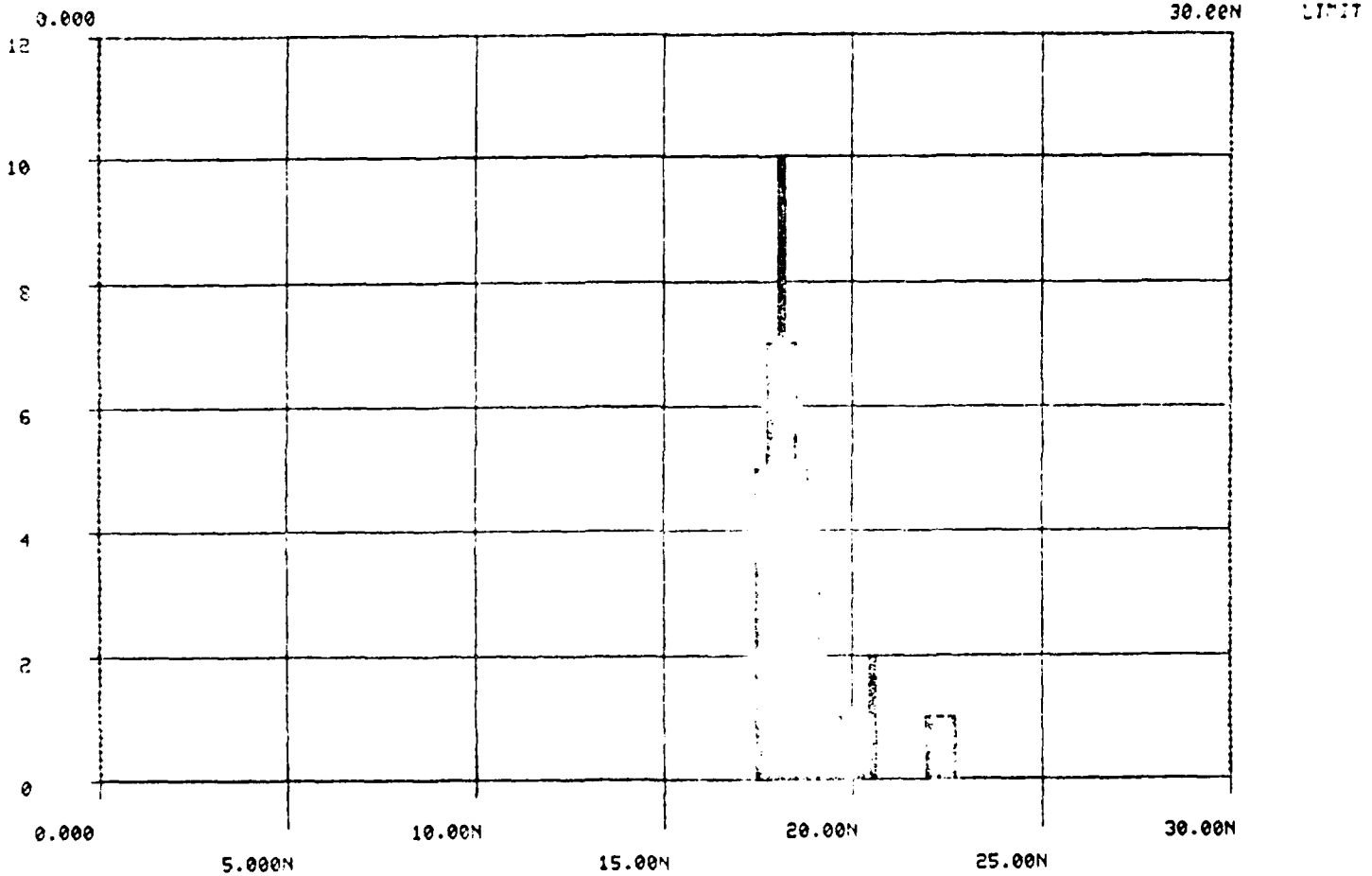
DISPLAY

LOW VALUE = 14.36494N HIGH VALUE = 21.41585N SAMPLES = 45

TOTAL

LOW VALUE = 14.36494N HIGH VALUE = 21.41585N SAMPLES = 45

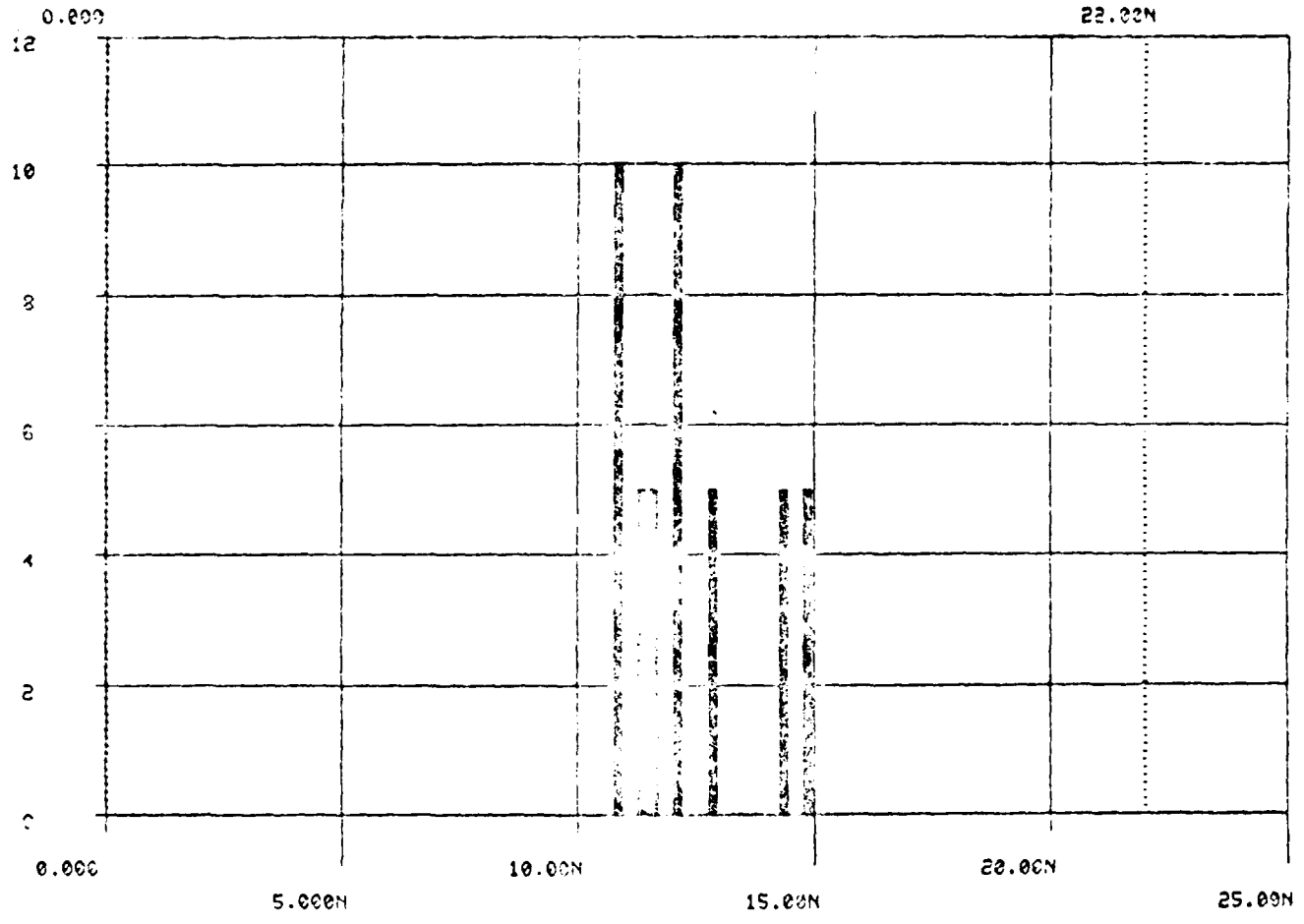
VALUE AT 5 FROM D3459.LOG:JED 13:38:38 17 DEC 80
TPHL AT VCC=4.5V DEVICE TYPE 54S08



TPHL @ +25 DEG C

		DISPLAY			
LOW VALUE =	17.5315BN	HIGH VALUE =	22.5459BN	SAMPLES =	45
		TOTAL			
LOW VALUE =	17.5315BN	HIGH VALUE =	22.5459BN	SAMPLES =	45

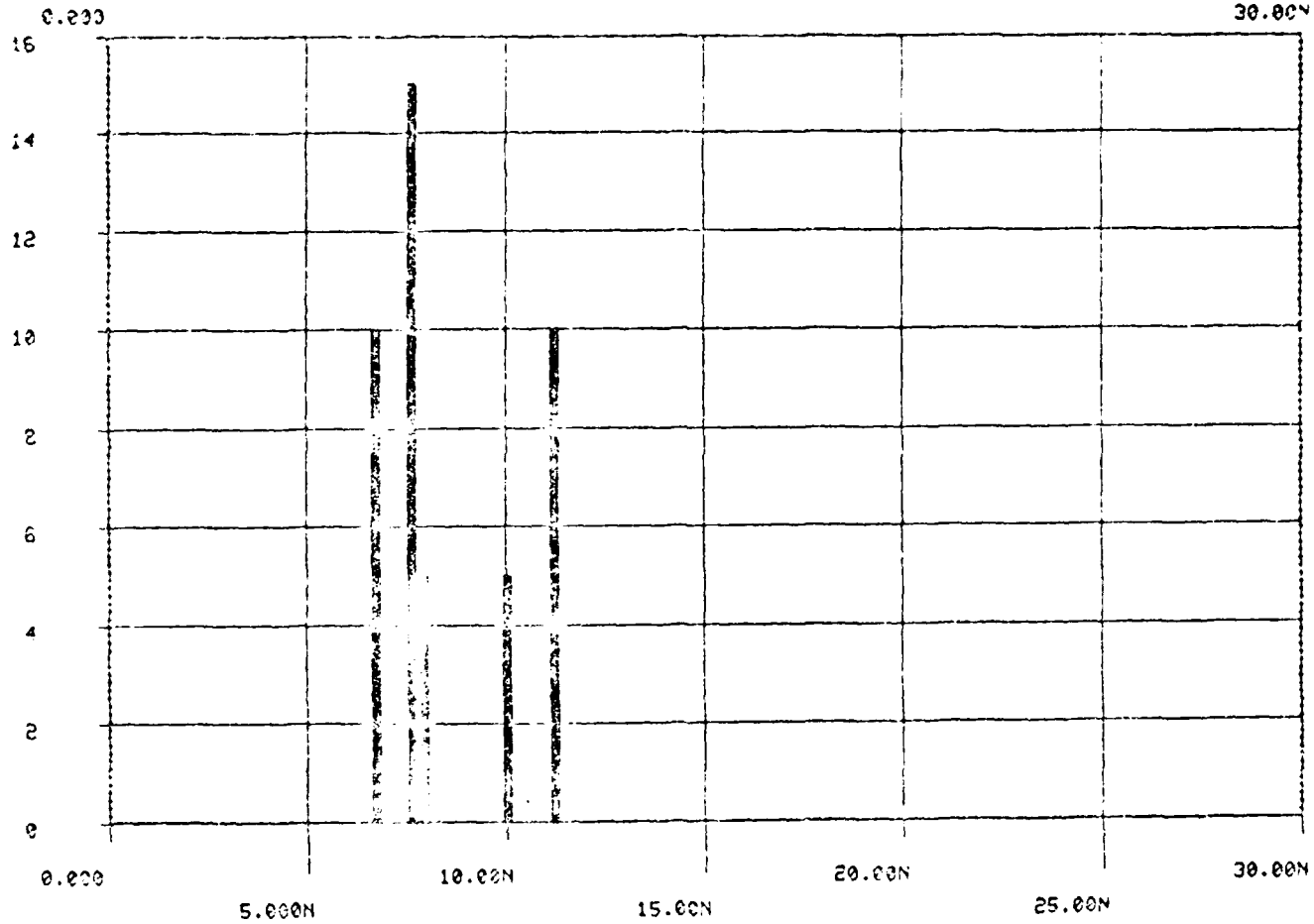
VALUE AT 5 FROM D4450.LOG:JED 14:02:41 17 DEC 80
TPLH1 AT VCC=4.5V (TTL GATE ONLY) DEVICE TYPE 55450



TPLH1 @ +25 DEG C

		DISPLAY			
LOW VALUE =	10.81000N	HIGH VALUE =	14.87000N	SAMPLES =	45
		TOTAL			
LOW VALUE =	10.81000N	HIGH VALUE =	14.87000N	SAMPLES =	45

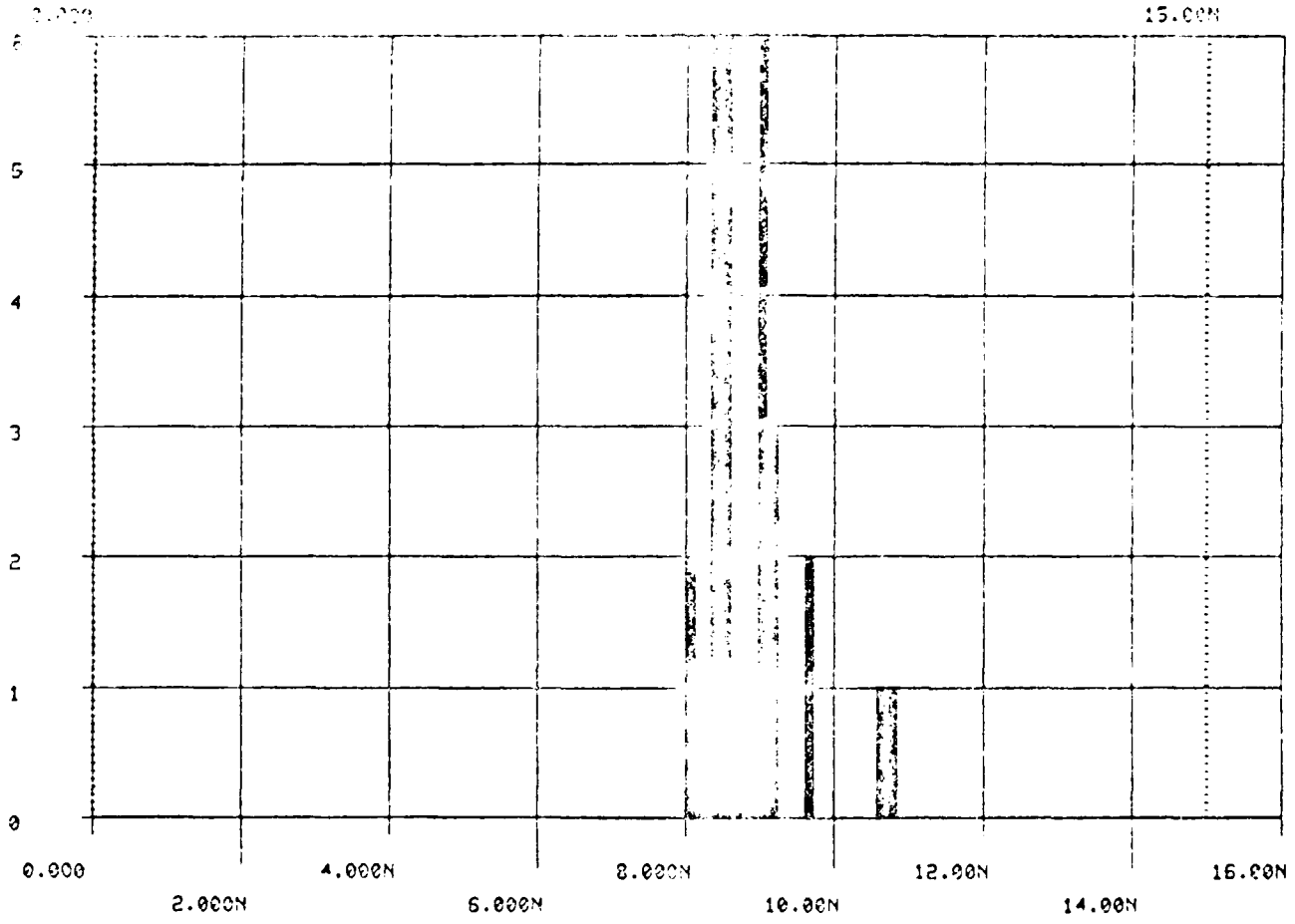
VALUE AT 5 FROM DC450.LOG1JED 14:00:32 12 DEC 90
TPHL2 AT VCC=4.5V (TTL GATE ONLY) DEVICE TYPE 55450



TPHL2 @ +25 DEG C

DISPLAY
LOW VALUE = 6.835001N HIGH VALUE = 11.30000N SAMPLES = 45
TOTAL
LOW VALUE = 6.835001N HIGH VALUE = 11.30000N SAMPLES = 45

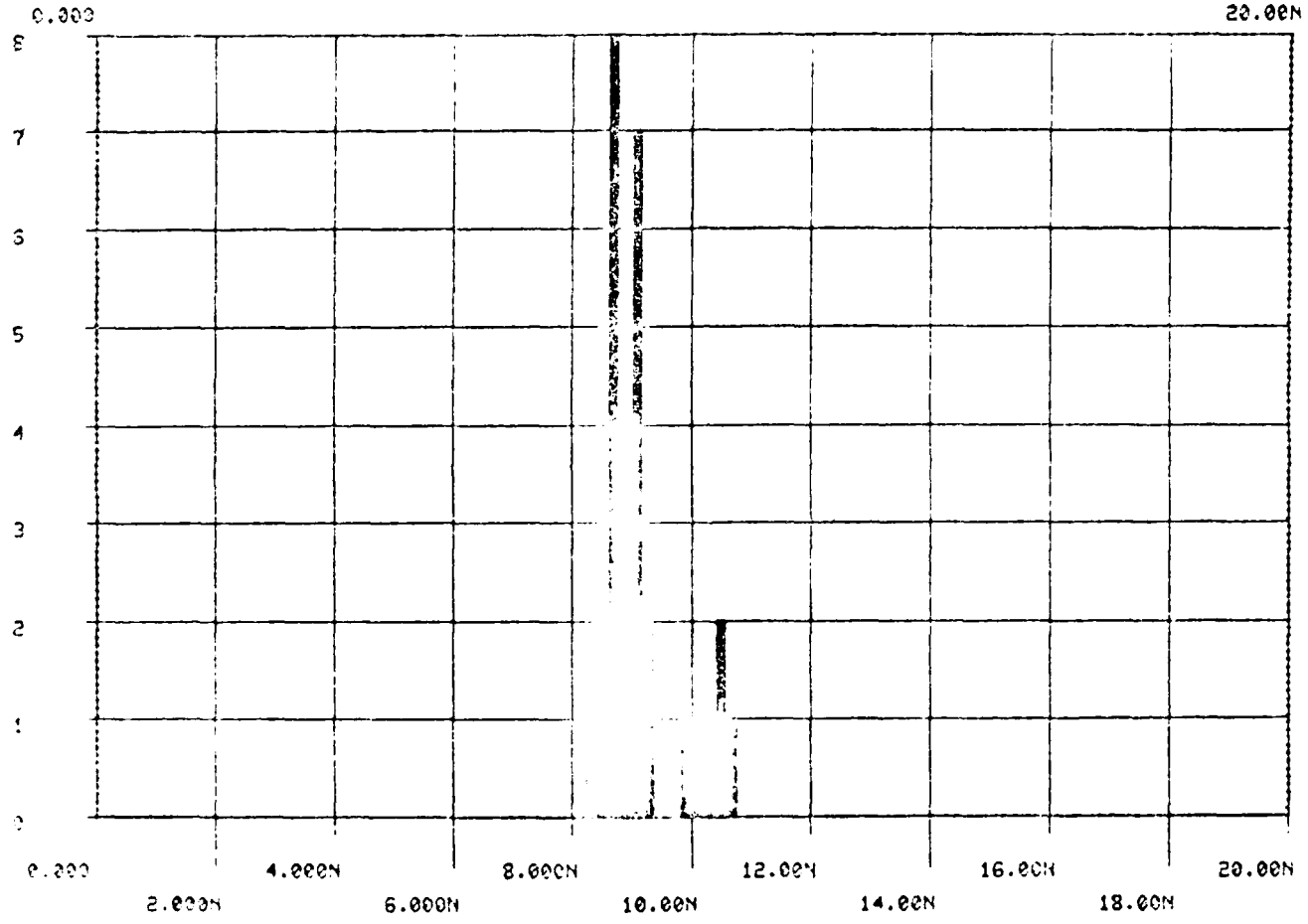
VALUE AT 5 FROM IR450.LOG:UED 15:34:27 17 DEC 80
tD-DELAY TIME AT IB=60-9,Ic=800-A DEVICE TYPE 554508



tD-DELAY TIME @ +25 DEG C

		DISPLAY			
LOW VALUE =	8.050001N	HIGH VALUE =	10.77000N	SAMPLES =	30
		TOTAL			
LOW VALUE =	8.050001N	HIGH VALUE =	10.77000N	SAMPLES =	30

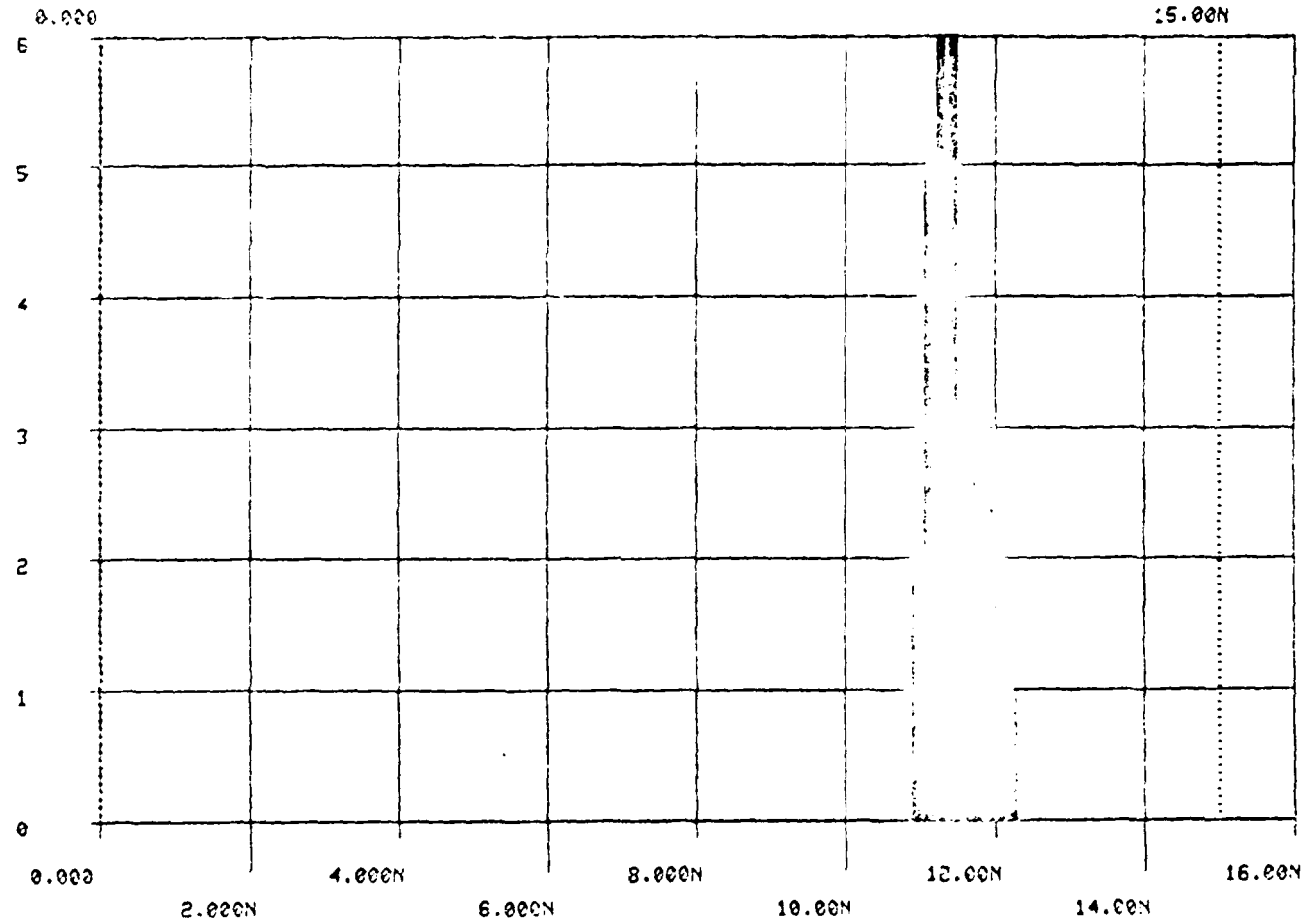
VALUE AT 5 FROM D4450.LOG:JED 15:39:27 17 DEC 80
tR-RISE TIME AT Ib=20mA,Ic=200mA DEVICE TYPE 554503



tR-RISE TIME @ +25 DEG C

DISPLAY
LOW VALUE = 8.400001N HIGH VALUE = 10.78000N SAMPLES = 30
TOTAL
LOW VALUE = 8.400001N HIGH VALUE = 10.78000N SAMPLES = 30

VALUE AT 5 FROM DP450.LOG:JED 15:44:48 17 DEC 80
tS-STORAGE TIME AT Ib=20mA,Ic=200mA DEVICE TYPE 5545OB



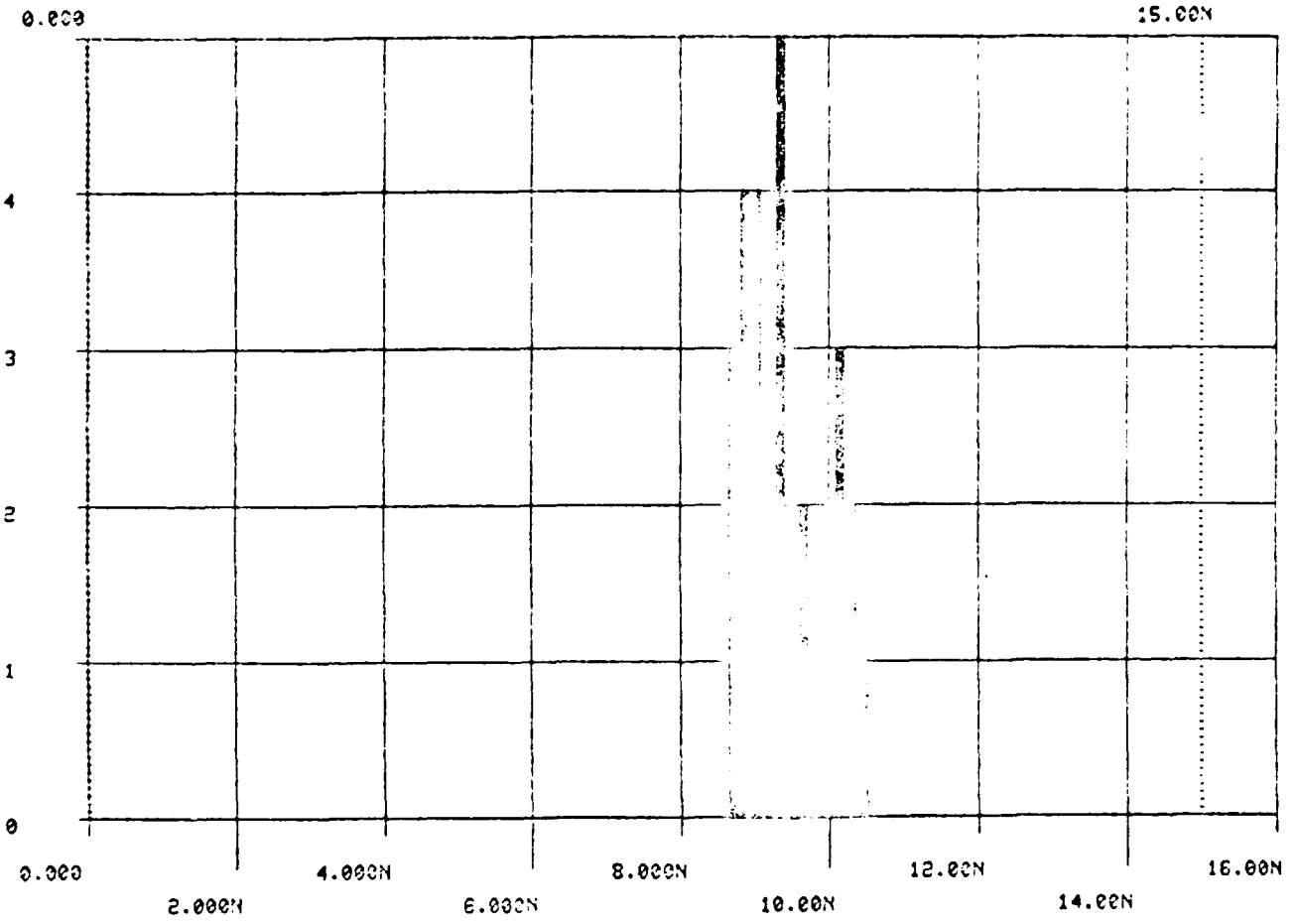
tS-STORAGE TIME @ +25 DEG C DISPLAY

LOW VALUE = 10.97000N HIGH VALUE = 12.1[illegible]00N SAMPLES = 29

TOTAL

LOW VALUE = 10.97000N HIGH VALUE = 111.4200N SAMPLES = 30

VALUE AT S FROM D0480.LOG:JED 15:51:34 17 DEC 80
tF-FALL TIME AT Ib=30-A,Ic=200mA DEVICE TYPE 554502

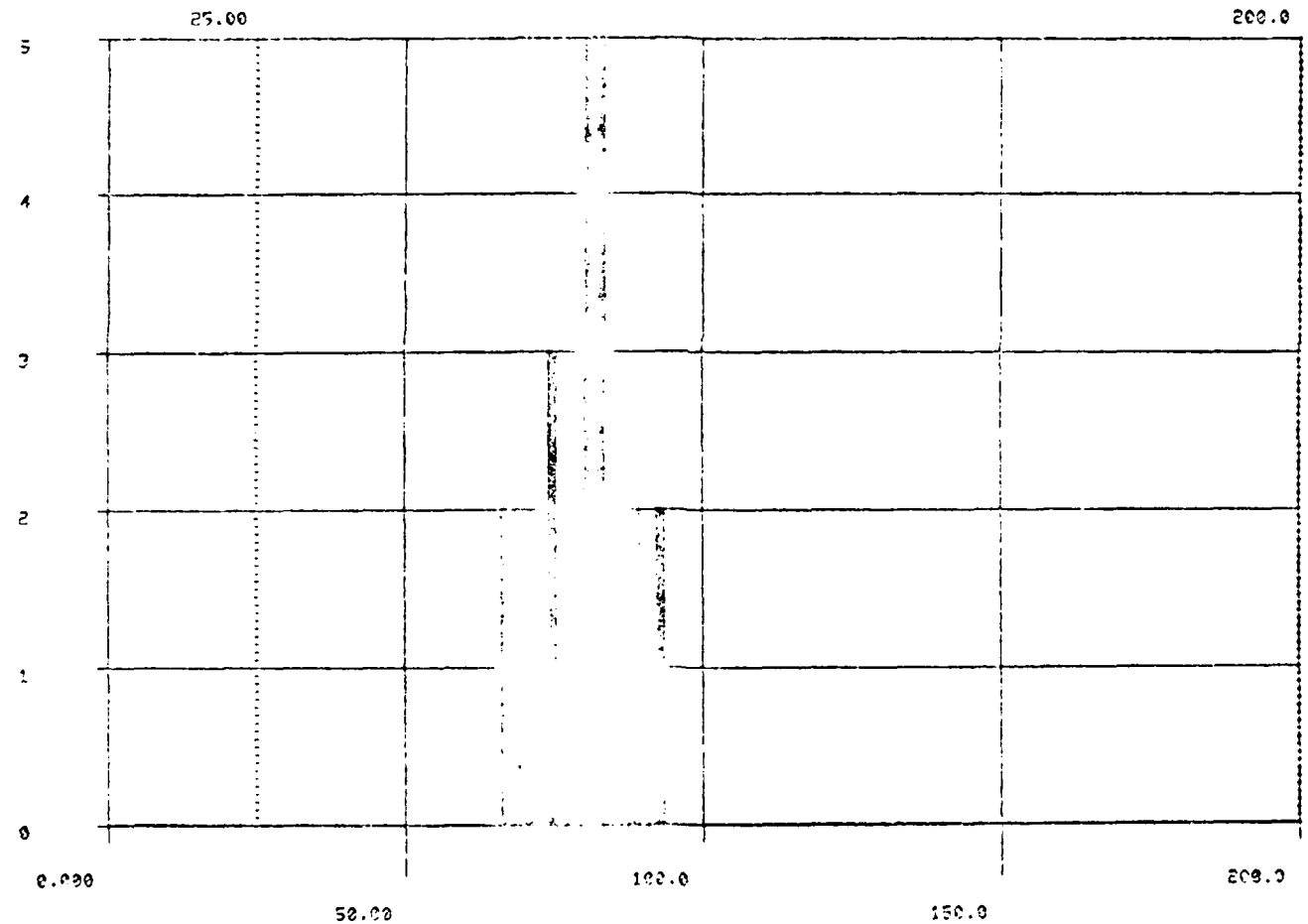


III-41

tF-FALL TIME @ +25 DEG C

	DISPLAY				
LOW VALUE =	8.670002N	HIGH VALUE =	10.51003N	SAMPLES =	30
	TOTAL				
LOW VALUE =	8.670002N	HIGH VALUE =	10.51003N	SAMPLES =	30

VALUE AT 5 FROM DP4501.LOG:JED 09:20:16 17 DEC 80
HFE1 AT Vce=3V,Ic=100mA DEVICE TYPE 5545OB

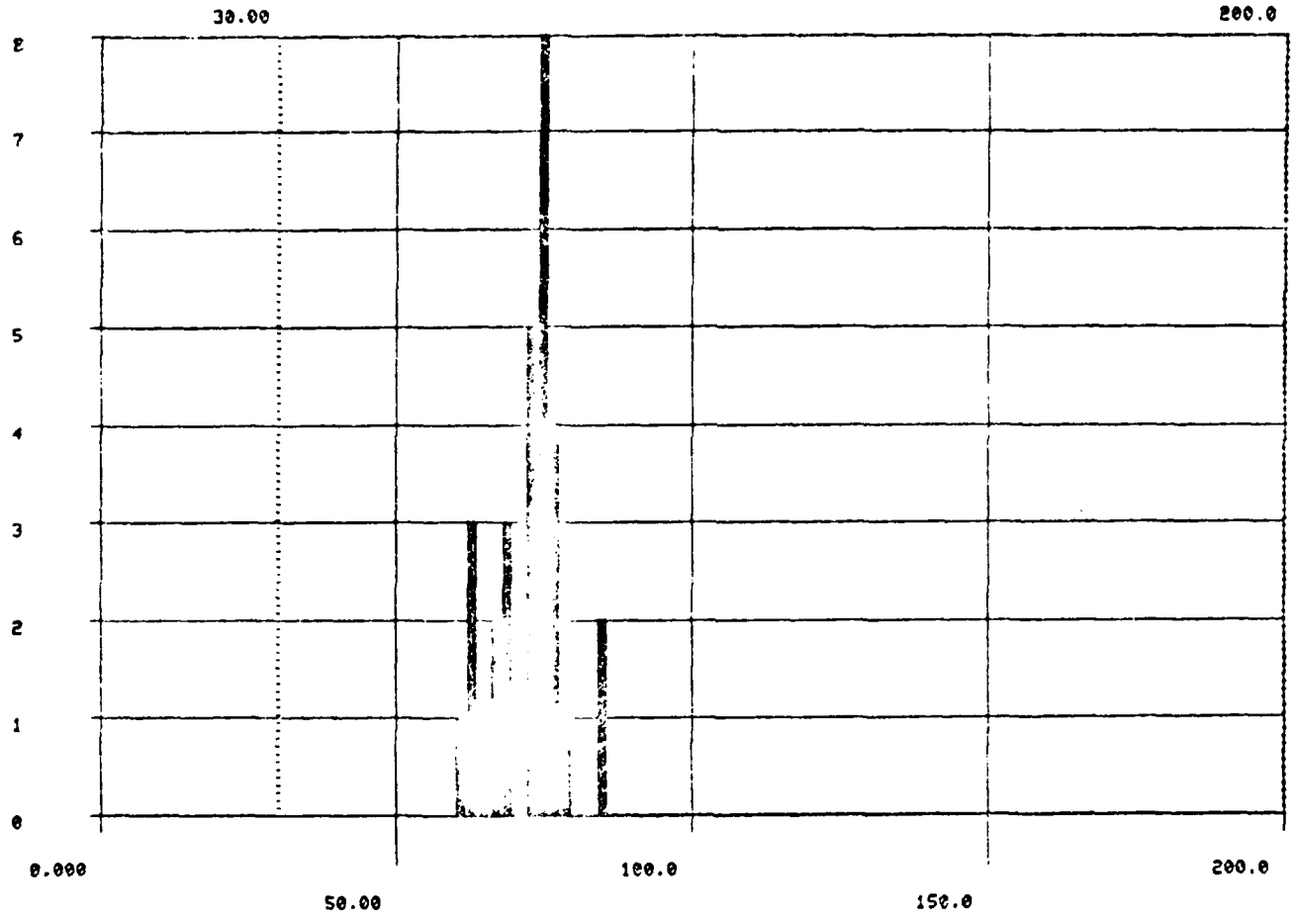


HFE1 @ +25 DEG C

LOW VALUE =	67.45000	HIGH VALUE =	93.40000	SAMPLES =	30
LOW VALUE =	67.45000	HIGH VALUE =	93.40000	SAMPLES =	30

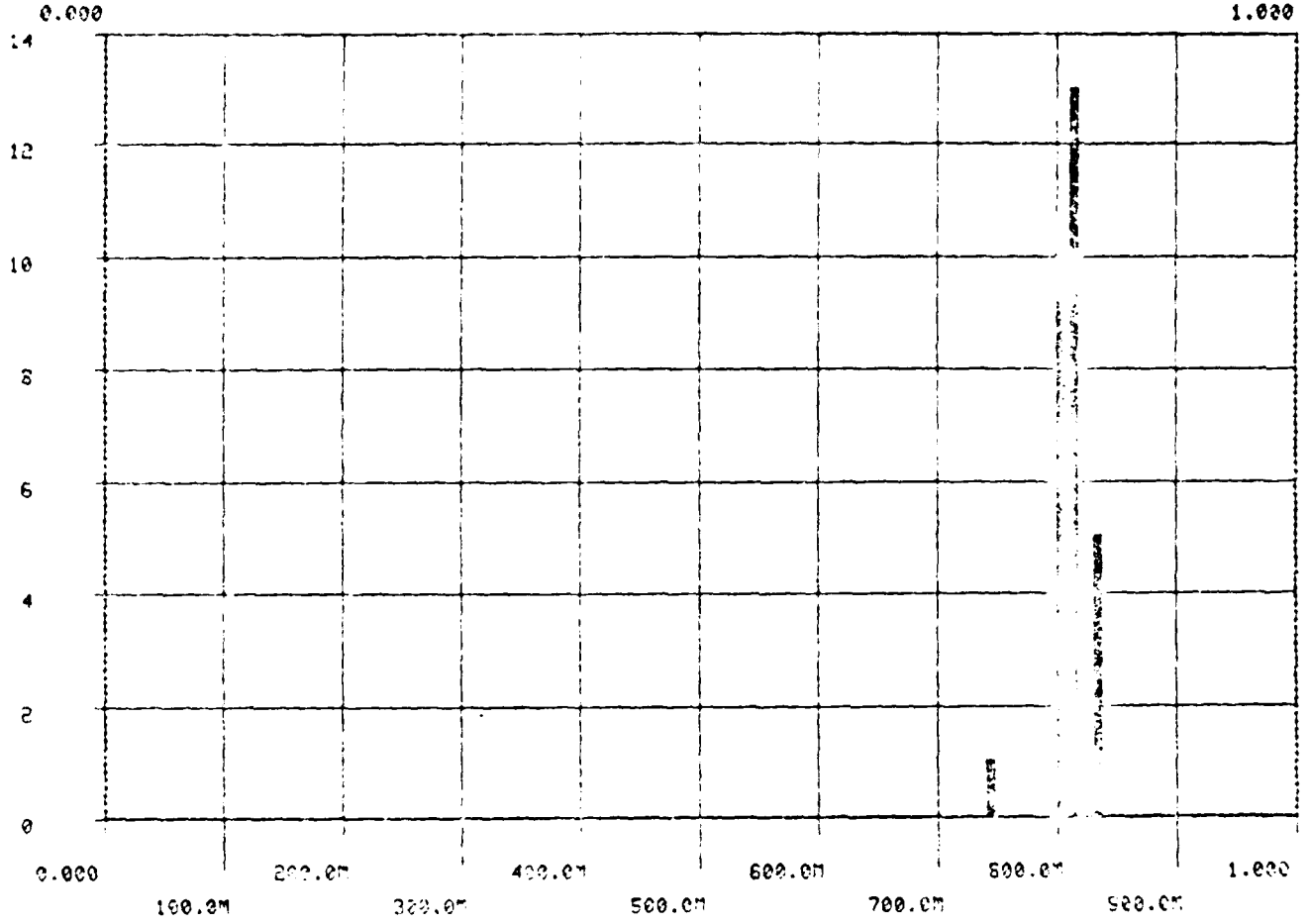
DISPLAY TOTAL

VALUE AT S FROM DP4502.LOG:JED 09:27:56 17 DEC 82
hFE2 AT Vce=3V,Ic=300mA DEVICE TYPE 55450B



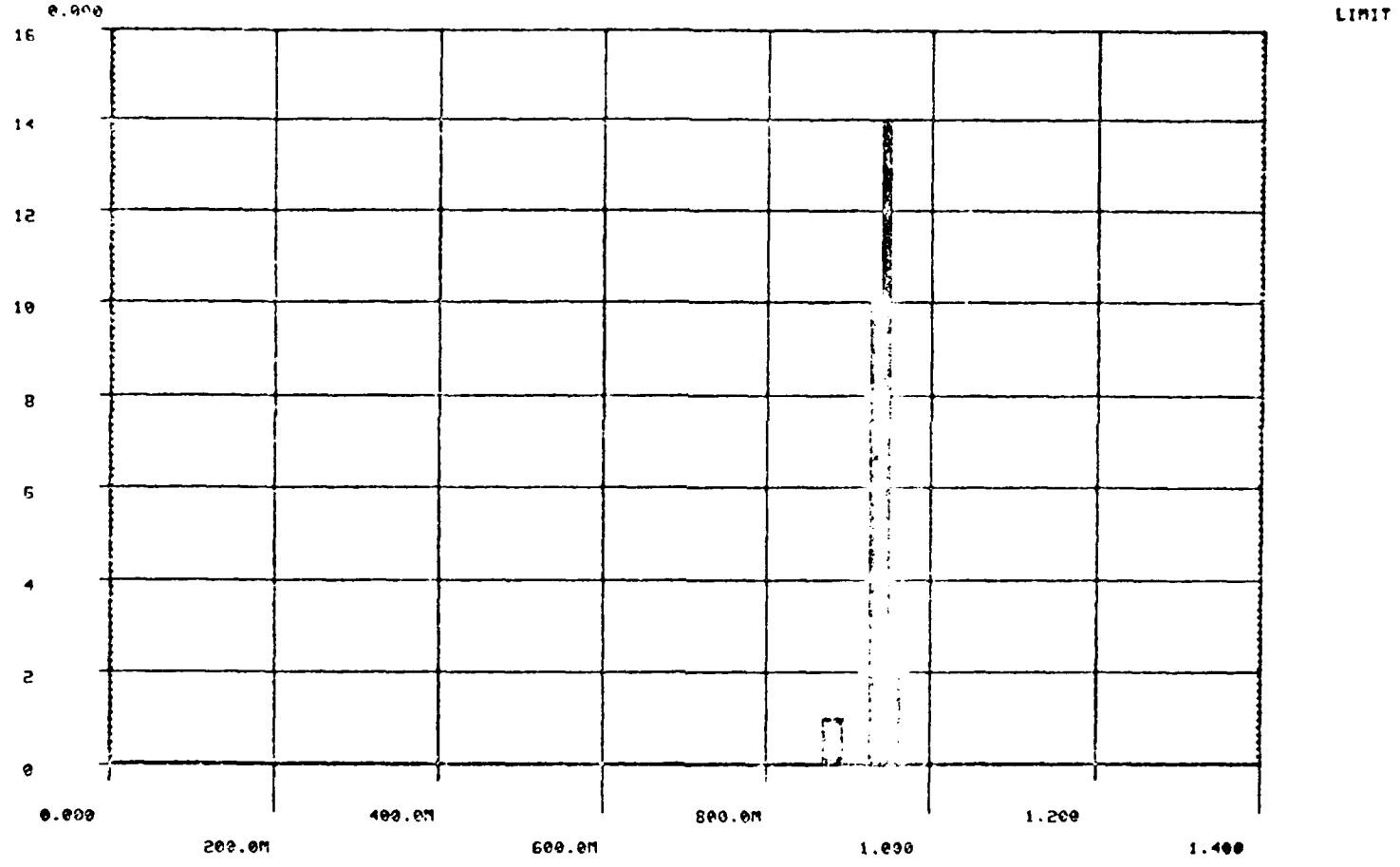
		DISPLAY			
LOW VALUE =	61.89000	HIGH VALUE =	85.19000	SAMPLES =	30
		TOTAL			
LOW VALUE =	61.89000	HIGH VALUE =	85.19000	SAMPLES =	30

VALUE AT 5 FROM DG450.LOG:JED 09:13:45 19 DEC 88
VBET AT Ib=10mA,Ic=100mA DEVICE TYPE 554508



DISPLAY
LOW VALUE = 742.2000M HIGH VALUE = 830.9999M SAMPLES = 30
TOTAL
LOW VALUE = 742.2000M HIGH VALUE = 830.9999M SAMPLES = 30

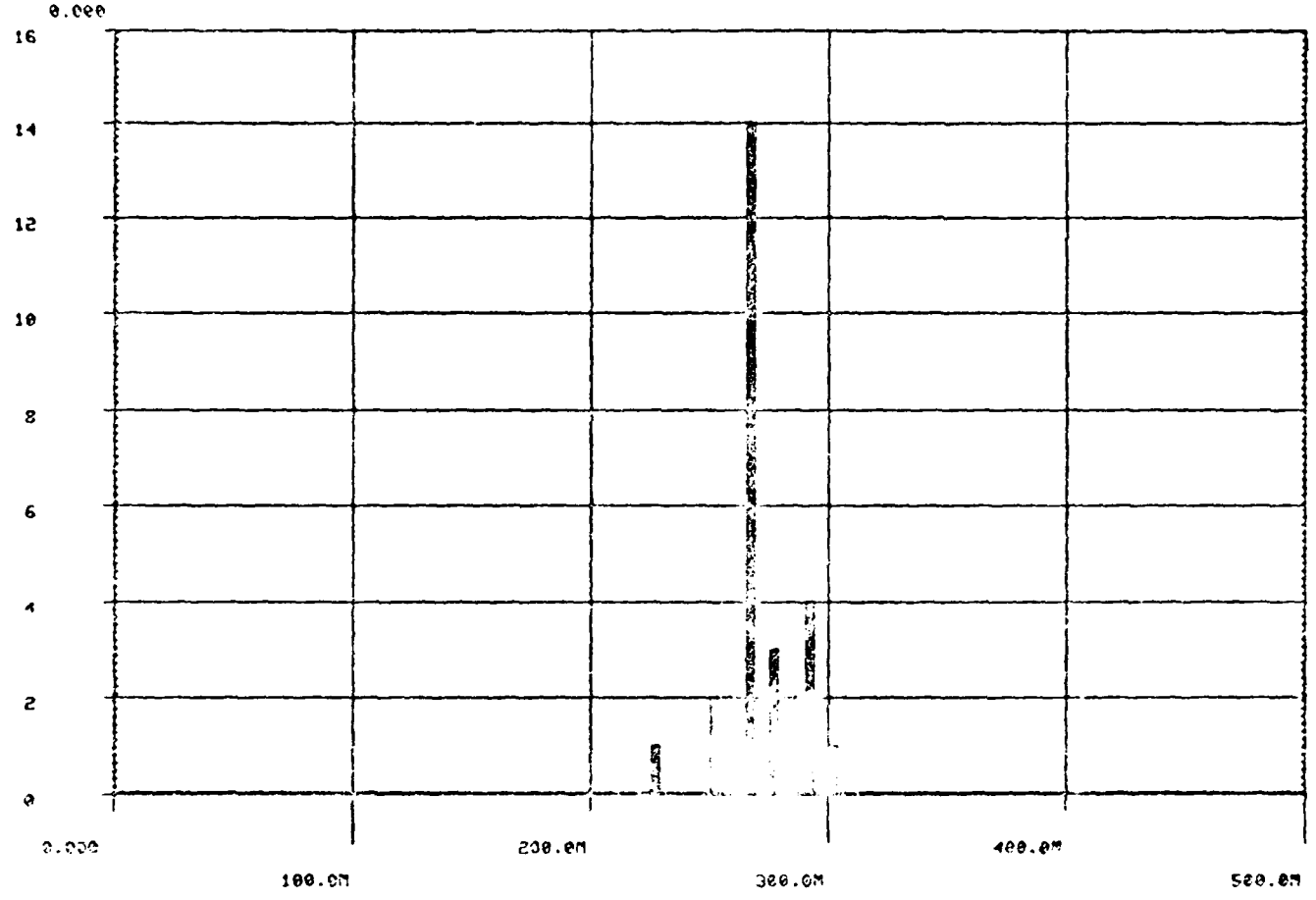
VALUE AT 5 FROM 2L456A.LOG;JED 14:11:50 19 DEC 88
VBE2 AT Ib=DC=A,Ic=DC=A DEVICE TYPE SS4503



VBE2 0 +25 DEG C

		DISPLAY			
LOW VALUE =	869.1000M	HIGH VALUE =	957.9000M	SAMPLES =	30
		TOTAL			
LOW VALUE =	869.1000M	HIGH VALUE =	957.9000	SAMPLES =	30

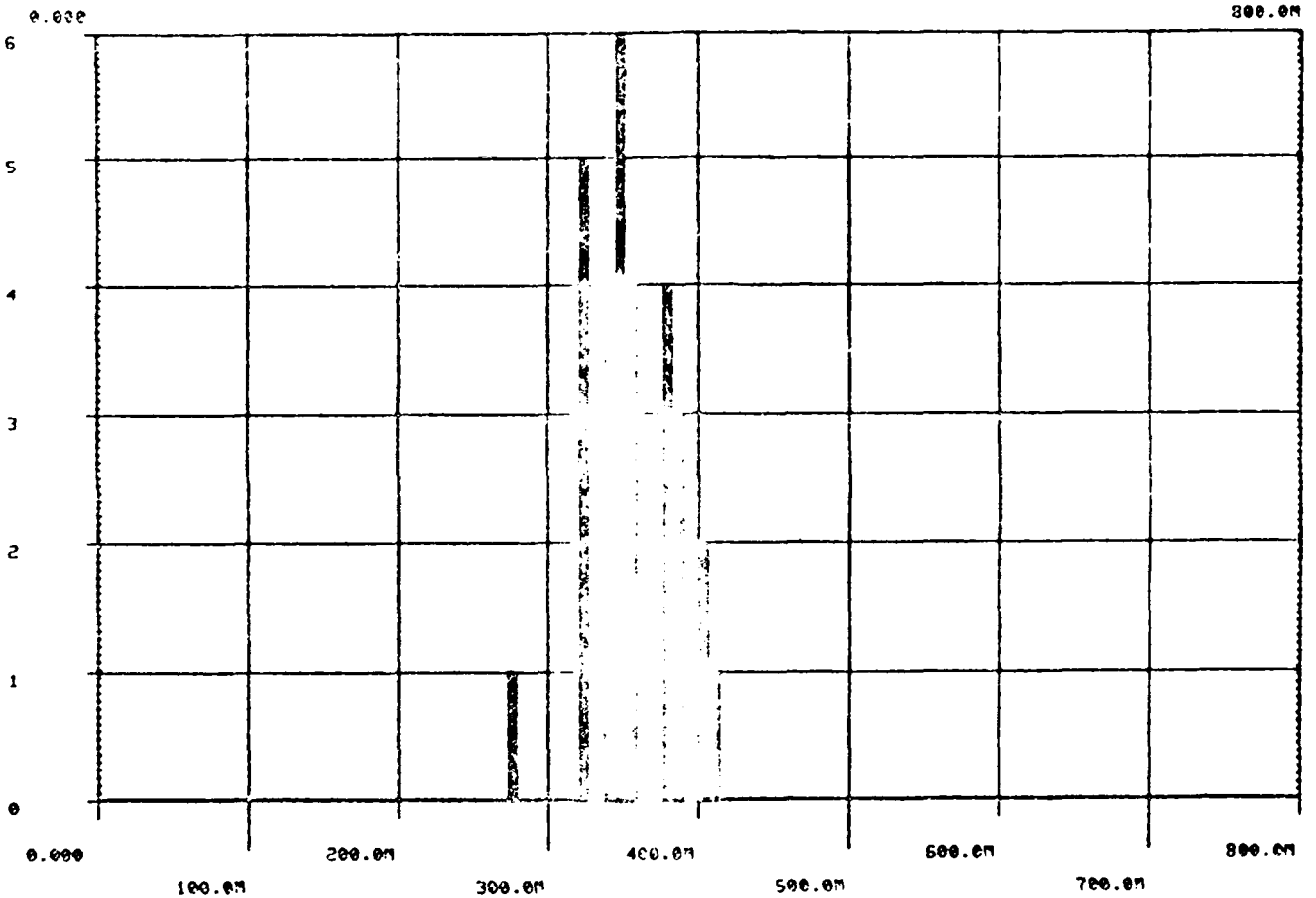
VALUE AT S FROM DI450.LOGIJED 13:56:26 19 DEC 80
VCEsati AT Ib=10mA,Ic=100mA DEVICE TYPE 55450B



VCEsati C +25 DEG C

		DISPLAY			
LOW VALUE =	227.1000M	HIGH VALUE =	323.2200M	SAMPLES =	30
		TOTAL			
LOW VALUE =	227.1000M	HIGH VALUE =	303.2000M	SAMPLES =	30

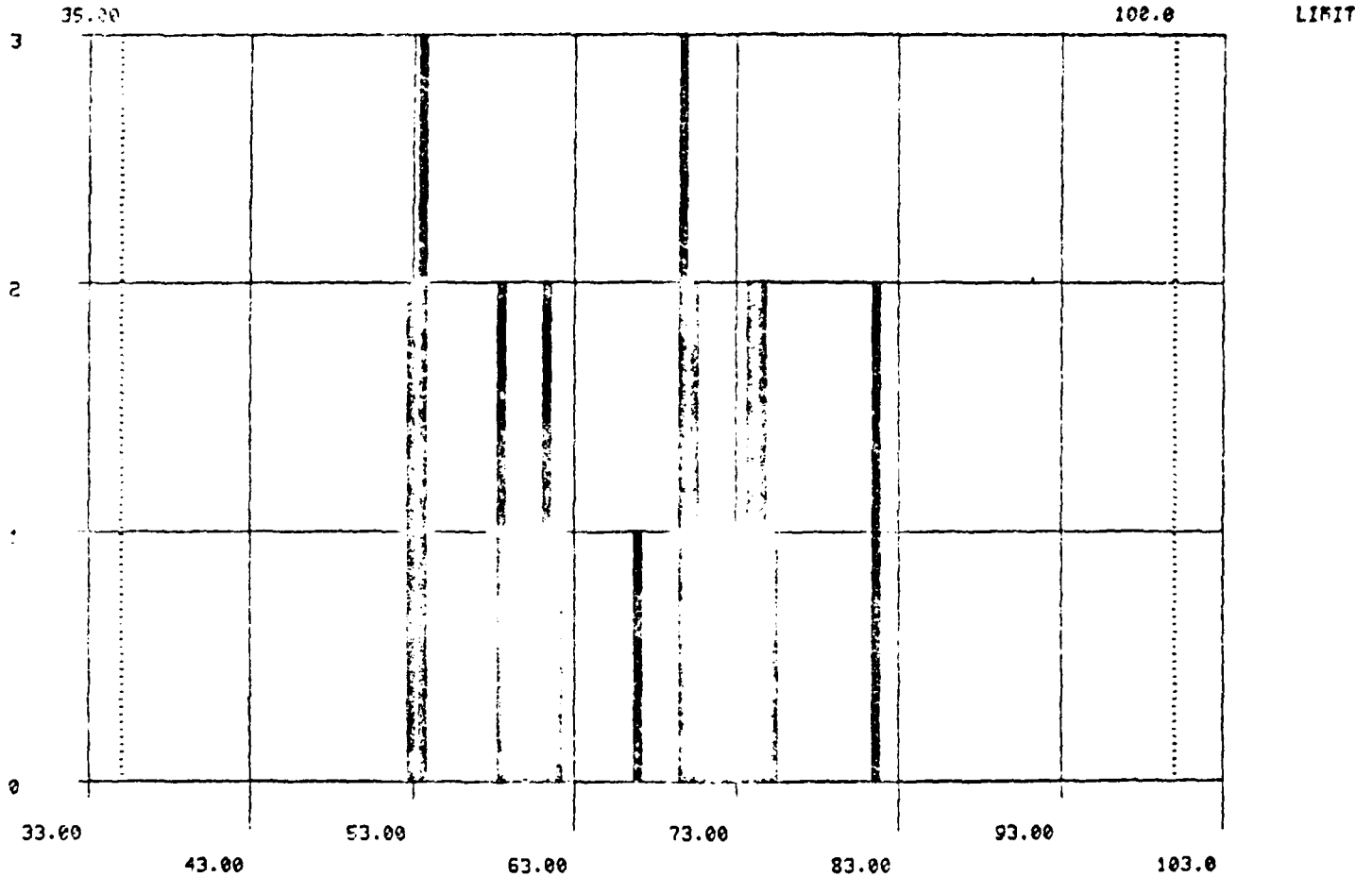
VALUE AT 5 FROM DJ450.LOG:UED 14:04:03 19 DEC 89
VCEsat2 AT Ib=30mA,Ic=300mA DEVICE TYPE 5545OB



VCEsat2 @ +25 DEG C

		DISPLAY			
LOW VALUE =	275.9000M	HIGH VALUE =	415.5000M	SAMPLES =	30
		TOTAL			
LOW VALUE =	275.9000M	HIGH VALUE =	415.5000M	SAMPLES =	30

VALUE AT 5 FROM D6450.LOG:JED 14:40:08 17 DEC 80
VCB01 AT Ic=100uA DEVICE TYPE 5962-8

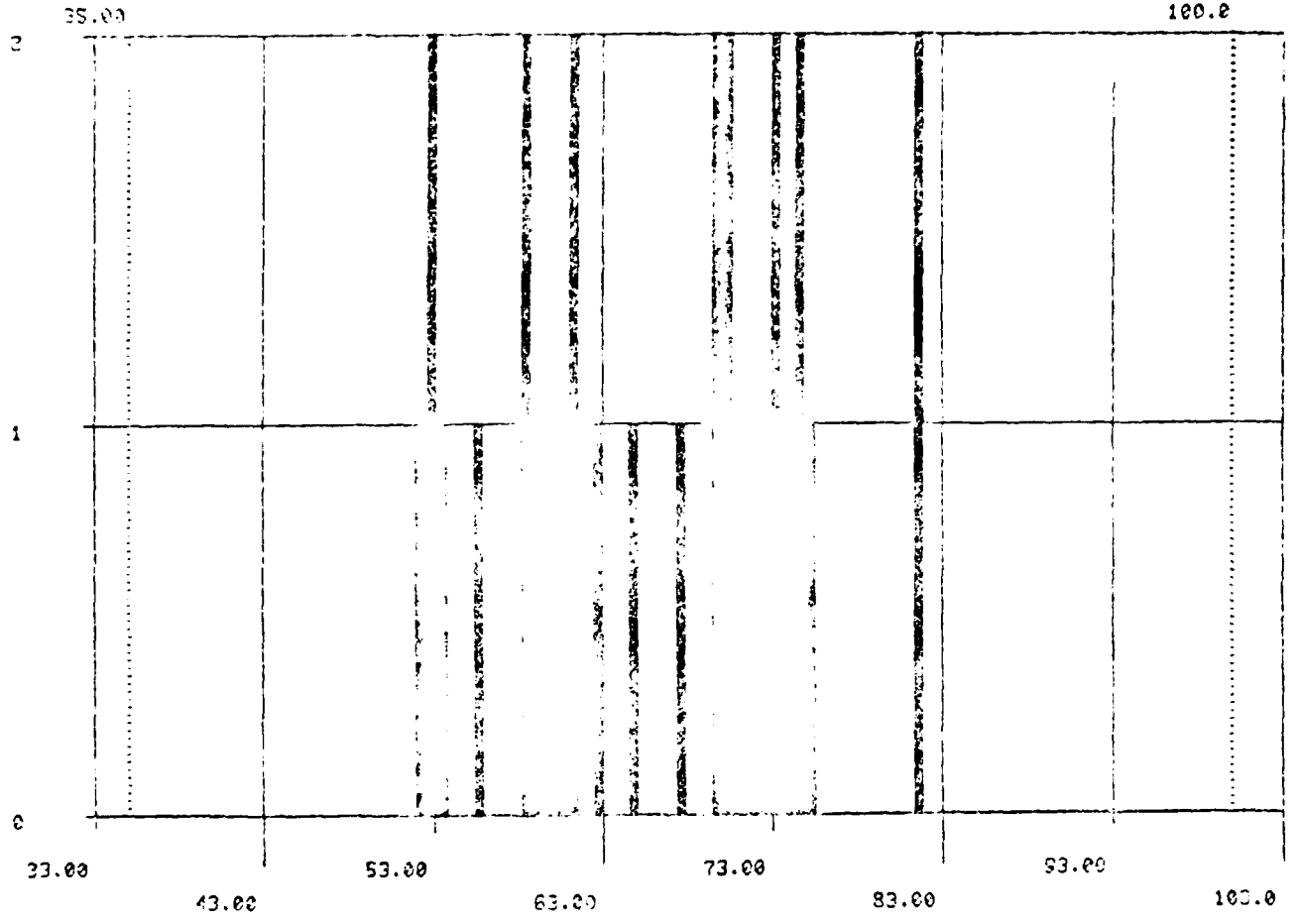


VCB01 @ +25 DEG C

LOW VALUE =	52.85000	HIGH VALUE =	81.95000	SAMPLES =	30
LOW VALUE =	52.85000	HIGH VALUE =	81.95000	SAMPLES =	30

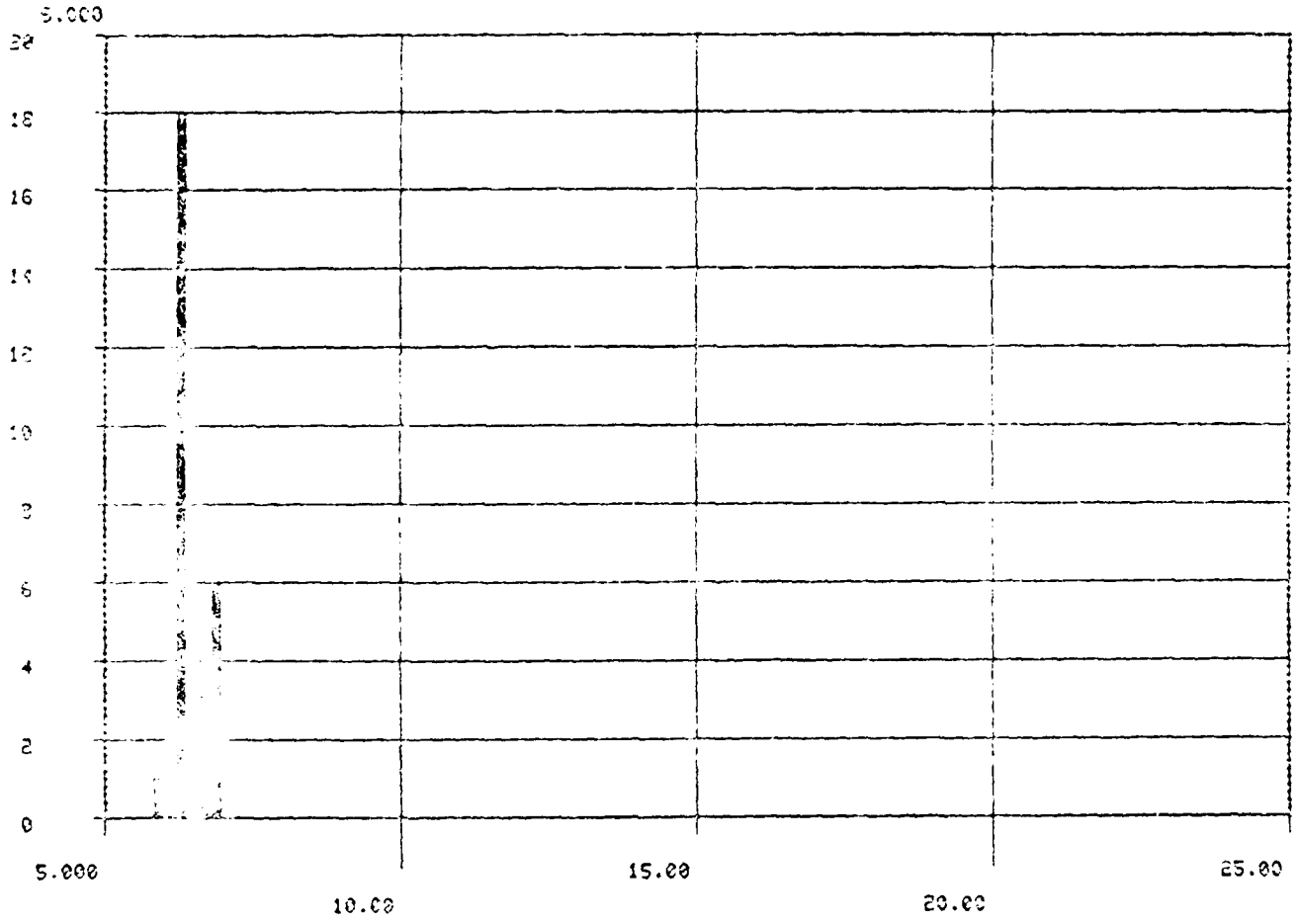
DISPLAY TOTAL

VALUE AT 5 FROM DT450.LOG:JED 14:48:55 17 DEC 80
VCER1 AT Ic=100uA,Rbe=500 ohms DEVICE TYPE 554503



LOW VALUE =	52.35000	DISPLAY HIGH VALUE =	81.75000	SAMPLES =	30
LOW VALUE =	52.35000	TOTAL HIGH VALUE =	81.75000	SAMPLES =	30

VALUE AT 5 FROM D2450.LOG:JED 14:59:47 17 DEC 80
VEBO AT Ie=100uA DEVICE TYPE 554008



VEBO @ +25 DEG C

		DISPLAY			
LOW VALUE =	5.995000	HIGH VALUE =	6.030000	SAMPLES =	30
		TOTAL			
LOW VALUE =	5.995000	HIGH VALUE =	6.030000	SAMPLES =	30

SECTION IV

MEMORY CORE DRIVERS

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SECTION IV

MEMORY CORE DRIVERS
MIL-M-38510/130

4.1 Introduction

The 55325/326/327 family of memory core drivers is the first line of core drivers to be characterized for RADC. Based on high previous utilization of these devices in military systems, both Texas Instruments and Fairchild Semiconductor recommended characterization of these devices. It is expected, however, that usage in new military systems will be on a decline. Table 4-1 gives some specifics on the devices tested and their relationship to the military slash sheet device types.

Table 4-1 Table of Device Types Specified

Device Type	Generic Type	Manufacturer Symbol	Output Configuration
130-01	55325	F, T	Dual source and dual sink
130-02	55326	F, T	Quad sink
130-03	55327	F, T	Quad source

F = Fairchild Semiconductor (discontinued mid-1980)
T = Texas Instruments

The manufacturer symbol column reflects the source of the devices which were to be characterized. Other vendors produce the 55325 but were not included in the characterization effort since they did not express interest in the devices. Fairchild memory core drivers were characterized. These devices were discontinued by Fairchild after characterization. Texas Instrument's components were received too late to be characterized.

4.2 Description of Device Types

The 55325/326/327 family of devices provide 600 mA of source or sink capability for memory core driver applications. Block diagrams of the various devices are given in Figure 4-1, and detailed schematics are given in Figure 4-2. The input circuit of the core drivers is identical to that used in a standard TTL gate. However, the totem pole driver and the output stage are designed differently in order to deliver higher output currents, to provide level translation from standard TTL levels to higher output voltages, and to provide a method of controlling maximum output current.

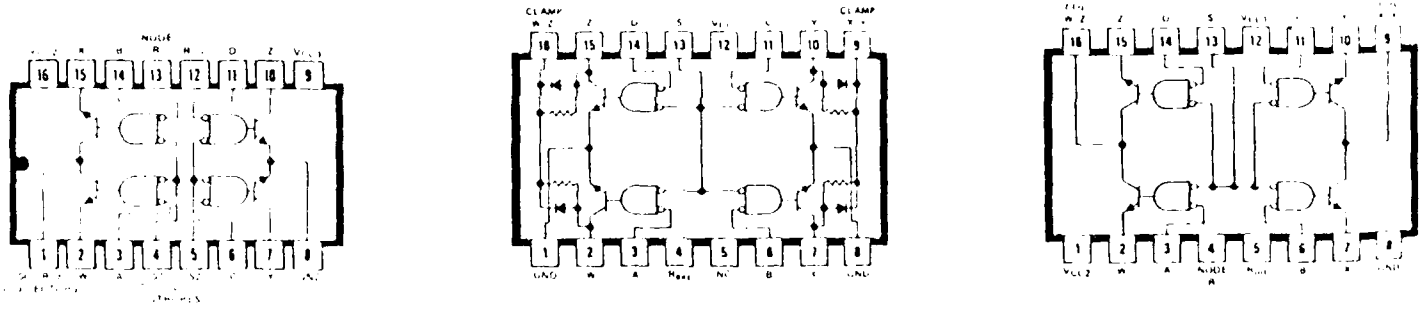
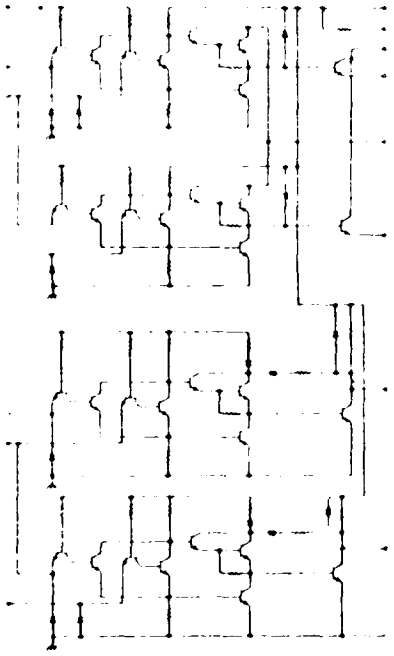
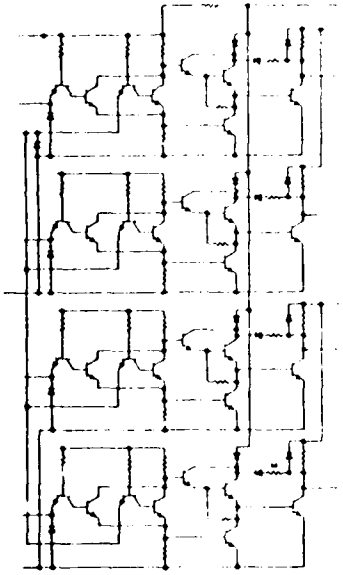


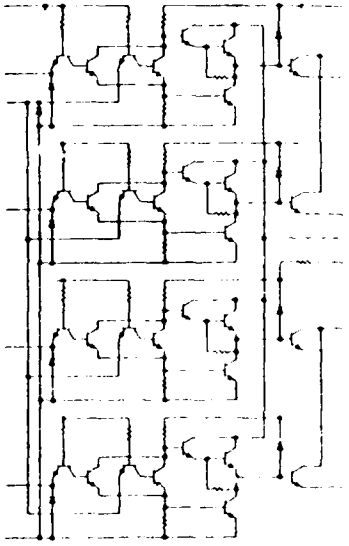
Figure 4-1 Block Diagrams, Memory Core Drivers



Device Type 01



Device Type 02



Device Type 03

Figure 4-2 Schematic Circuits, Memory Core Drivers

The primary difference between the 55325, 55326 and the 55327 memory core drivers is their output arrangement. The 55325 provides two source and two sink outputs. The 55326 furnishes 4 sink outputs and the 55327 has 4 "source outputs".

4.3 Test Development

The test development for memory core drivers was similar to the bench test development for peripheral drivers (see Section 3.3). V_{IH}, V_{IL}, V_{IK}, I_I, I_{IH}, I_{IL}, $I_{CC\ (off)}$, I_{CC1} and I_{CC2} are tested in much the same way as they are for standard TTL gates.

All other test parameters require special consideration, however, since they involve pulse measurement techniques or high speed switching of the devices under test.

A simplified schematic for the static test circuit is included in Figure 4-3. (The actual test box developed contained all of its own loads, drive signals and power supplies.

Schematics of the switching time test circuits are included in figures 4-4, 4-5, 4-6 and 4-7. Automatic tests were not implemented for characterization of this device family.

4.4 Test Results and Data

A total of 24 memory core drivers were bench tested at $T_A = 25°C$. Sample test data of devices parameters is included in Table 4-2. Testing the 55325 family of devices is straightforward, requiring simple load circuits and TTL type test conditions. Testing is complicated, however, by the large combination of input and output configurations required by the device under test.

Tests that require unusual techniques are described below:

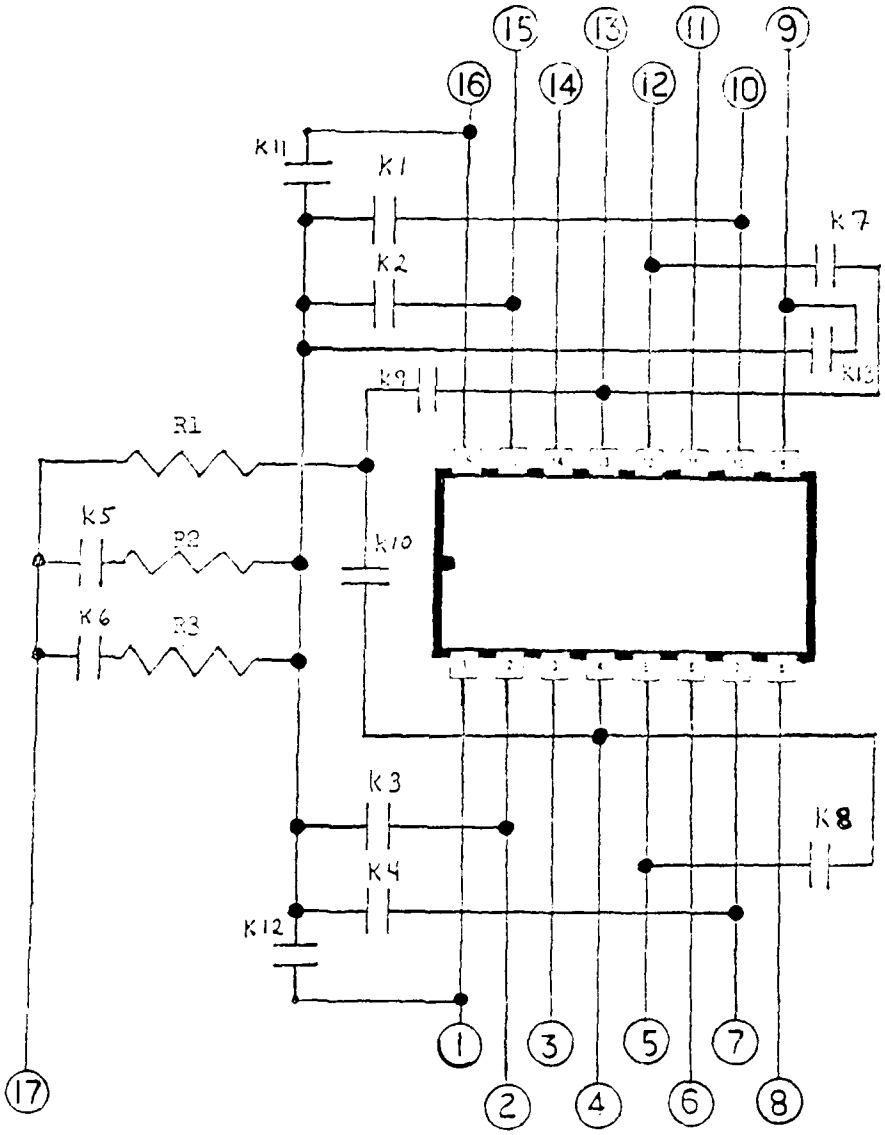
Saturation "Voltage", $V_{(SAT)}$

$V_{(SAT)}$ is measured using pulse techniques. The manufacturers data sheet specifies that $t_w = 200$ us with a duty cycle of $\leq 2\%$. The devices were measured over a range of repetition rates and duty cycles. The measured $V_{CE(SAT)}$ was relatively insensitive to changes in both test conditions. (Refer to figure 4-8.)

This parameter must be measured at the DUT pins to minimize measurement error.

Parameter	Test Conditions	Test Pin #	SN1	SN2	SN3	SN4	SN5	SN6	SN7	SN8	SN9	SN10	SN11	SN12	SN13	Units
[illegible]	V_{cc1}=4.5V, V_{cc2}=24V	4	1.3	1.4	1.4	1.3	1.4	-	1.3	1.3	1.4	1.4	1.4	1.4	1.3	V
		3,14	1.4	1.3	1.3	1.4	1.4	-	1.3	1.4	1.4	1.3	1.4	1.3	1.3	
		5	1.36	1.36	1.34	1.35	1.32	1.29	1.35	1.35	1.36	1.36	1.34	1.35	1.35	
		9	1.36	1.36	1.34	1.35	1.34	1.30	1.33	1.35	1.35	1.35	1.34	1.35	1.36	
		6	1.34	1.33	1.34	1.32	1.36	1.27	1.34	1.34	1.34	1.33	1.35	1.34	1.35	
		11	1.37	1.34	1.35	1.36	1.37	1.30	1.36	1.37	1.36	1.34	1.34	1.36	1.35	
I_{OFF}	V_{cc1}=4.5V, V_{cc2}=24V	1	2.9	3.1	3.5	3.1	3.0	-	3.2	3.1	3.4	3.2	15.2	5.5	2.8	uA
V_{OH}	V_{cc1}=4.5V, V_{cc2}=24V	7	23.1	23.2	23.2	23.1	23.1	23.1	23.2	23.2	23.1	23.1	23.0	23.2	23.1	V
		10	23.1	23.2	23.2	23.2	23.1	-	23.2	23.3	23.2	23.1	23.1	23.2	23.2	
I_{IL}	V_{cc1}=5.5V, V_{cc2}=24V	3	0.83	0.75	0.75	0.75	0.77	0.64	0.77	0.78	0.80	0.72	0.83	0.79	0.85	mA
		14	0.86	0.76	0.77	0.77	0.77	0.64	0.78	0.80	0.81	0.74	0.85	0.81	0.87	
		9	0.90	0.76	0.77	0.76	0.79	0.62	0.79	0.81	0.82	0.75	0.86	0.80	0.88	
		11	0.93	0.83	0.84	0.84	0.84	0.65	0.84	0.86	0.89	0.81	0.92	0.89	0.94	
		4	1.72	1.51	1.52	1.52	1.54	1.27	1.55	1.58	1.62	1.47	1.68	1.60	1.73	
		5	1.71	1.51	1.51	1.52	1.54	1.26	1.54	1.59	1.62	1.47	1.68	1.59	1.72	

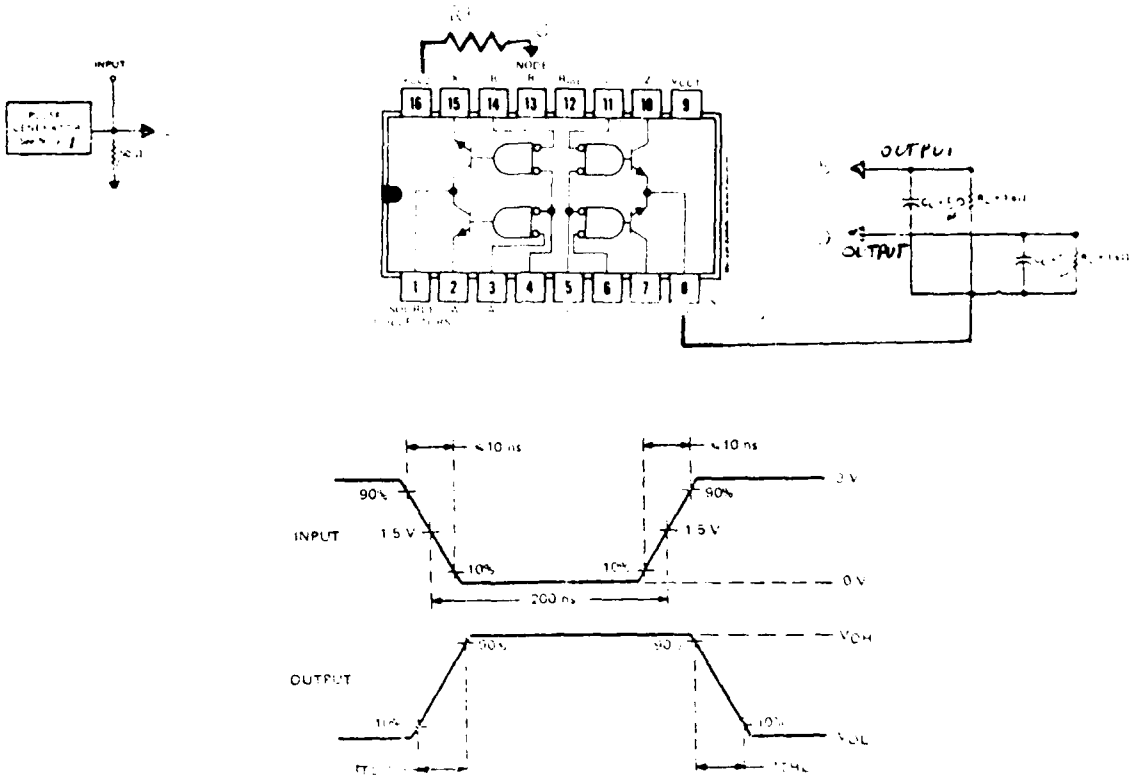
TABLE 4-2. Sample Test Data, 55325.



Notes: 1. All relays are in the de-energized position.

2. R1 = 360 ohms ±5% carbon.
3. R2 = 39 ohms ± 5% carbon.
4. R3 = 22 ohms ± 5% carbon.

Figure 4-3 Simplified Static Test Circuit Diagram for Memory Core Drivers

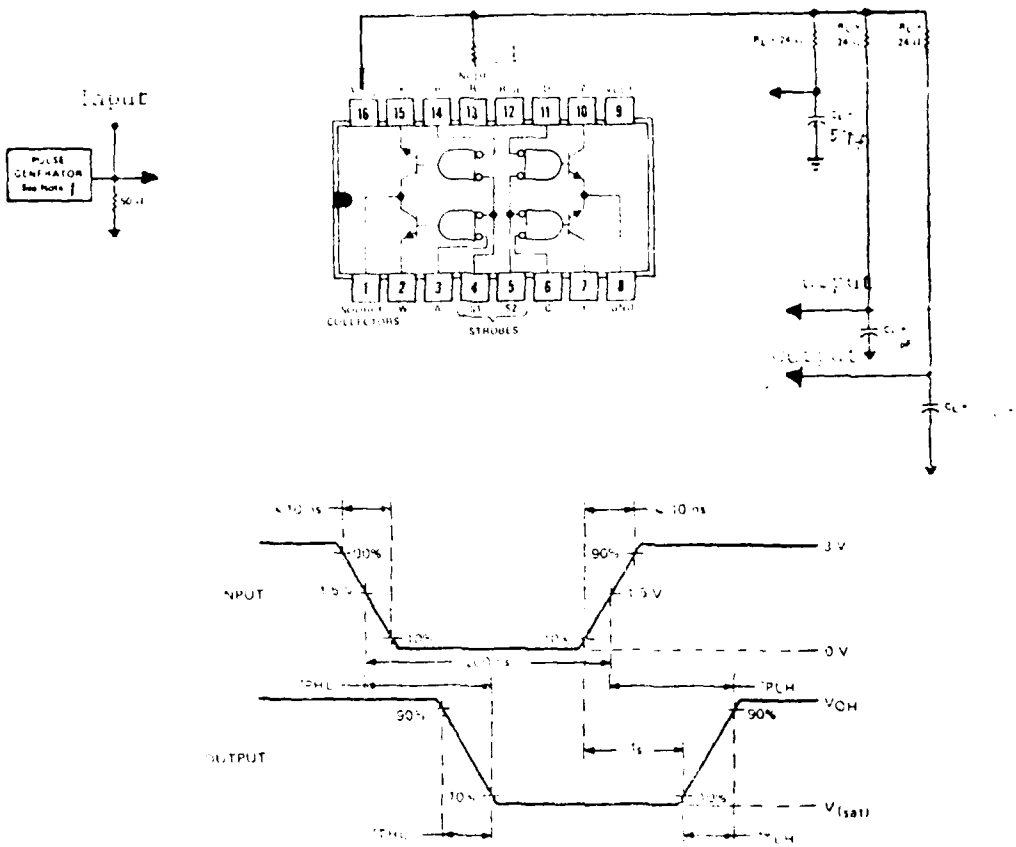


Notes: 1. The pulse generator has the following characteristics:

PRR = 0.2uS, t_p = 200nS, $Z_{out} \approx 50\ \Omega$.

2. R_L = 1Kohm ± 5% carbon.
3. C_L = 50pF ± 5%, including probe and jig capacitance.
4. R_1 = 300 ohms ± 5% carbon.

Figure 4-4 Switching Time Test Circuit for Device Type 01

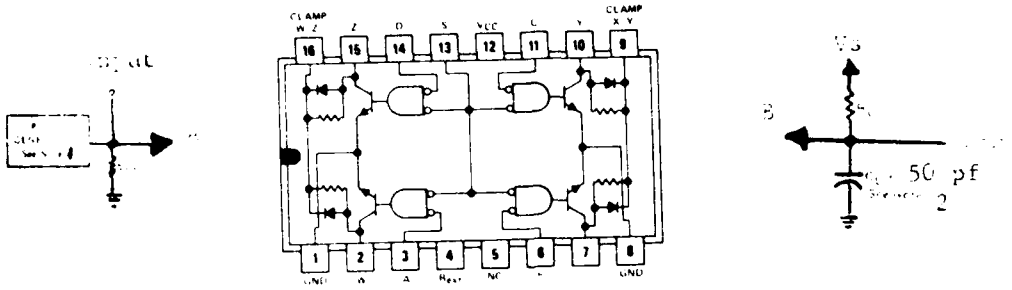


Notes: 1. The pulse generator has the following characteristics:

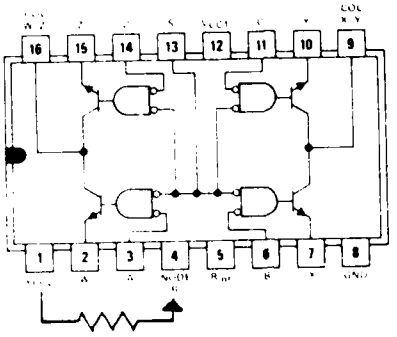
PRR = [illegible], t_p = 200nS, Z_{out} 50

2. R_L = 24Ω ± 5% carbon.
3. C_L = 50pF ± 5%, including probe and jig capacitance.
4. R_1 = [illegible]ohms ± 5% carbon.

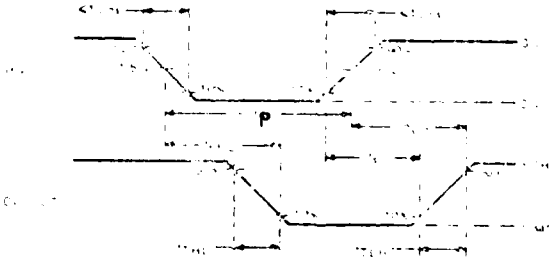
Figure 4-1 Switching Time Test Circuit for Device Type 01



Device Type 02



Device Type 03

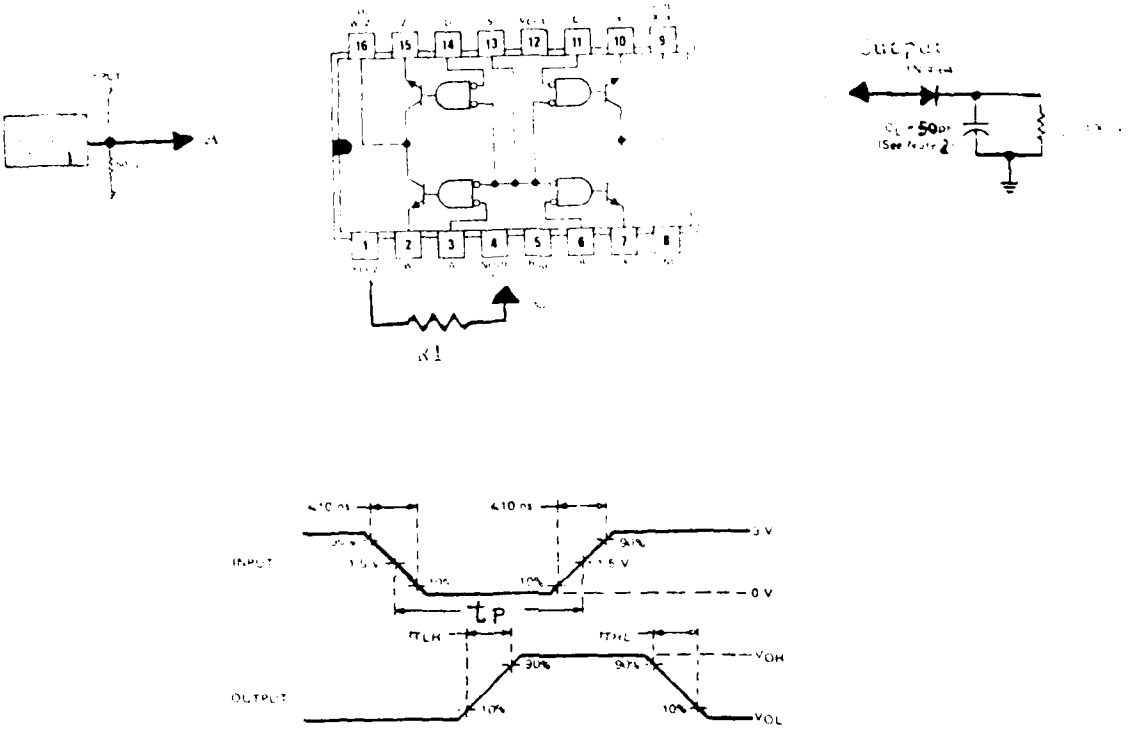


Notes: 1. The pulse generator shall have the following characteristics:

$Z_{out} \approx 50$ ohms - For testing V_{OH} (after switching)
PRR = 12.5kHz, t_p = 40uS - For all other tests.
PRR = 0.2uS, t_p = 200nS.

2. C_L = 50pF ± 5% (including jig and probe capacitances).
3. R_L = 4[illegible] ohms ± 5% carbon for V_{OH} tests. For all other tests R_L = 22 ohms ± 5% carbon.
4. Connect V3 to V(Clamp) for device type 02. For device type 03, connect V3 to VCC2.
5. R1 = 3[illegible] ohms ± 5% (device type 03 only).

Figure 4-6 Switching Time Test Circuit for Device Types 02 and 03



Notes: 1. The pulse generator shall have the following characteristics:

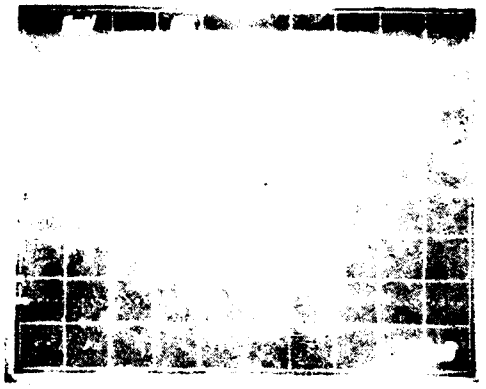
$Z_{out} \approx 50$ ohms, PRR = 0.2mS, t_p = 200nS

2. C_L = 50pF ± 5% (including jig and probe capacitances).
3. R_L = 100 ohms ± 5% carbon.
4. R1 = 360 ohms ± 5% carbon.

Figure 4-7 Switching Time Test Circuit for Device Type 03

$V_{(SAT)}$ = .38
Rep Rate = 10
Duty Cycle = 2%

$V_{(SAT)}$ = .389
Rep Rate = 10 m
Duty Cycle = 10%



$V_{(SAT)}$ = .38
Rep Rate = 10
Duty Cycle = 20%

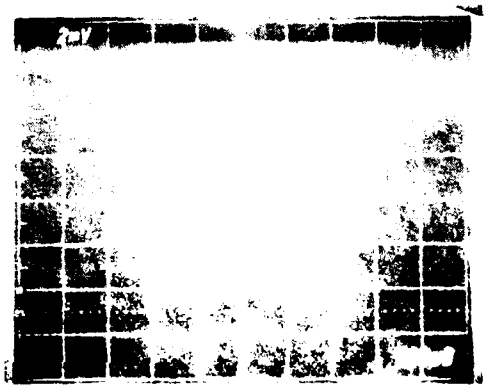


Figure 4-8 Saturation Voltage vs Duty Cycle for 5532S Device

Switching characteristics T_{PLH}, T_{PHL}, T_{PLH}, T_{PHH}

The following guidelines were used to ensure accurate and repeatable switching time measurements:

1. Test circuits were built on ground planes to minimize induced noise through signal returns and to minimize circuit inductances. High frequency wiring techniques were used throughout.

2. All power supply voltage pins were bypassed as close to the device under test (DUT) as possible. All supply lines were then checked for noise with the DUT switching.

3. The total bandwidth of the oscilloscope mainframe, plug ins, and probes were selected and verified to provide an overall oscilloscope measurement bandwidth of 350 MHz. This translates to an oscilloscope rise/fall time of 1 ns.

4. All probes were adjusted for proper compensation.

5. The time skew between channels on the oscilloscope was nulled out.

6. The input signal to the DUT was terminated to minimize line reflections. The input signal line was made as short as possible to shorten the time frame during which any residual reflections might occur.

7. Supply voltages were carefully regulated to minimize switching time measurement errors due to supply voltage variation.

8. Load capacitance was adjusted for probe capacitance.

Most of the switching parameter results were as expected; however, one anomaly was discovered in T_{PHL} measurements at the source outputs for the >>325 devices. As shown in Figure 4-9, the high to low output transition shows a very high initial slope, but suddenly flattens out approximately 10 ns after the start of the output transition.

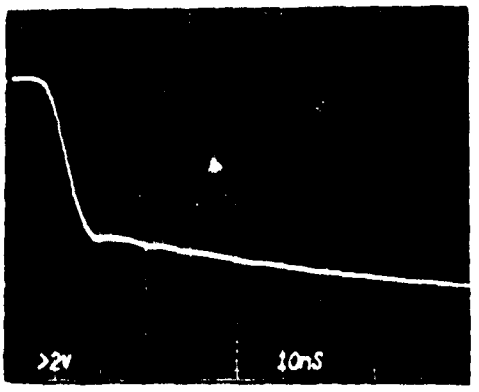


Figure 4-9A

T_{PHL} source output, >>325
Vendor A
C_L = 25 pF
R = 1 K

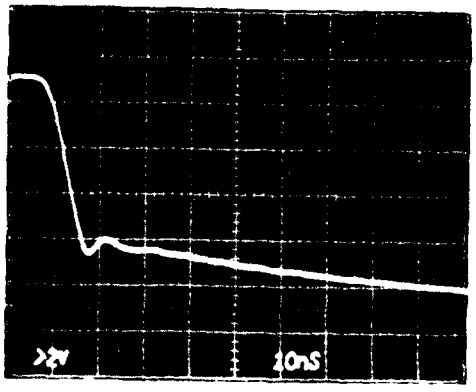


Figure 4-9B

I_{PHL} source output, 5532
Vendor B
C_L = 25 pF
R_L = 1 K

One possible explanation for this effect involves reverse recovery action in the output stage.

As shown in Figure 4-10 (the simplified schematic diagram), the source section of the 5532 consists of a standard TTL input followed by a high voltage totem pole driver and an emitter follower output. Assume that the input is initially in a logic low state. Q_5 is off, causing the Darlington pair (consisting of Q_3 and Q_4) to be on and Q_2 to be off.

Hence, Q_1 is conducting and the output is in a high state.

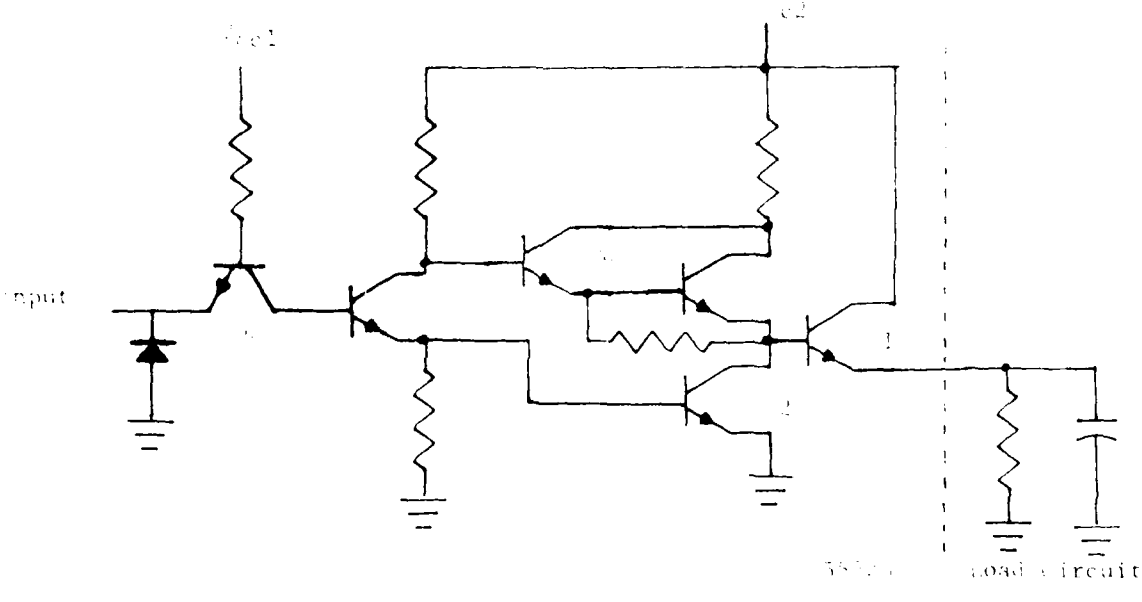


Figure 4-10 Simplified Source Section of 5532

If the input to the gate were to change from the low state to the high state, the collector of Q_1 will become forward biased, Q_3 will turn on, Q_3 and Q_4 will turn off, and Q_2 will start to conduct.

As the totem pole driver (consisting of Q_2, Q_3 and Q_4) changes state, the bias voltage across the emitter junction of Q_1 changes from the forward direction to the reverse direction. Reverse recovery action begins in the emitter of Q_1, tending to discharge C_L rapidly through the emitter of Q_1 and through Q_2. After recover, Q_1 is cut off and C_L is left to discharge through R_L. Hence, the output of the core driver shows a two slope transition. The steep initial transition is due to discharge of C_L primarily through Q_1, and the flatter portion of the transition occurs as C_L discharges through R_L.

A similar effect could occur with emitter breakdown of Q_1 during a high to low output transition. Further work is needed to investigate the exact cause.

4.6 Slash Sheet Development

The military specification (MIL-M-38510 slash sheet) on memory core drivers was developed in parallel with the characterization effort. As the test circuits and procedures were proofed out in the taking of device data, they were also incorporated into the slash sheet. With few exceptions, the proposed slash sheet Table I parameters and limits are the same as in the manufacturers data sheets. Limit changes were made only to switching parameters. An anomaly was observed in T_{THL} at the source outputs for the 55325. Further investigation is needed to fully understand the cause.

4.7 Conclusions and Recommendations

Twenty-four generic 55325 series memory core drivers were bench tested at GEOS. The devices tested in a predicatable fashion and within manufacturers limits except for selected switching time measurements. The data and slash sheet parameters and limits will be reviewed by interested manufacturers prior to issuance of MIL-M-38510/130.

SECTION V

CMOS MULTIPLYING D/A CONVERTERS

MIL-M-38510/127

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AD-A102 841 GENERAL ELECTRIC CO PITTSFIELD MA ORDNANCE SYSTEMS F/G 9/5
ELECTRICAL CHARACTERIZATION AND SPECIFICATION OF PERIPHERAL DRI--ETC(U)
MAY 81 J S KULPINSKI, T HACK, T SIMONSEN F30602-80-C-0057
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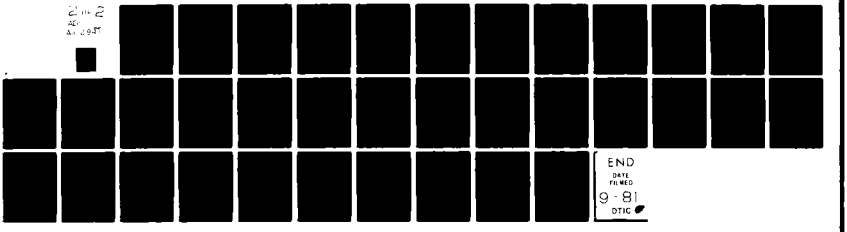

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SECTION V

MIL-M-38510/127

5.1 Introduction

CMOS multiplying digital to analog converters were initially introduced in late 1973 by Analog Devices. Since then these devices have been used in many applications and several other manufacturers have incorporated them into their product lines. Table 5-1 shows the CMOS multiplying DA converters to be specified in MIL-M-38510/127.

Table 5-1. Table of Device Types Specified.

Device Type	Generic Type	Manufacturer Code *	Multiplying D/A Converter Description
01	AD7523S	A,M	8-bit res., 8-bit lin.
02	AD7520U	A,M,I,N	10-bit res., 10-bit lin.
03	AD7521U	A,M,I,N	12-bit res., 10-bit lin.
04	AD7541T	A,I	12-bit res., 12-bit lin.
05	AD7541T	A,I	12-bit res., 12-bit lin.**
06	DAC1020LD	N	10-bit res., 10-bit lin.
07	DAC1220LD	N	12-bit res., 10-bit lin.
08	DAC1218LD	N	12-bit res., 12-bit lin.
09	DAC1220LD	N	12-bit res., 12-bit lin.**

*Manufacturer Code
A = Analog Devices
M = Micro Power
I = Intersil
N = National Semiconductor

**Best fit linearity. All others are specified with end-point linearity.

Later deleted in slash sheet per agreement reached at JEDEC JC-41 meeting, 12 Feb 81.

A recommendation for characterization and possible slash sheet action was made by the JC-41 Committee to RADC. Some device features which should sustain this recommendation are as follows:

1. First monolithic 10-bit D/A converter. (AD7520)

2. Many potential applications and user options.

3. Cost effective with other competing process technologies.

4. Device is sourced by several manufacturers.

5. Low power dissipation.

6. Usage in military systems is high.

5.2 Description of Device Types

This CMOS series of multiplying D/A converters are fabricated with a deposited thin film R-2R ladder over a CMOS integrated circuit. A functional schematic of a typical circuit is shown in Figure 5-1.

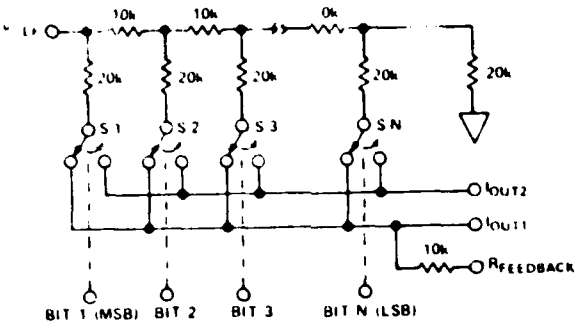


Figure 5-1. CMOS Multiplying D/A Converter

The R-2R ladder resistors consists of silicon-chromium material arranged to provide the network shown. In one vendor's design, these resistors have nominal values of 10 K ohms and 20 K ohms with an absolute temperature coefficient of approximately -300 ppm/oC and a tracking temperature coefficient of better than 1 ppm/oC.

When a voltage is applied to the reference terminal of the structure, the precision of the binary division of current is governed by the matching of the resistors and the drop across the associated switches. For proper operation the output terminals Iout1 and Iout2 should be as close to ground reference as possible. The CMOS switches of the integrated circuit structure are shown schematically in Figure 5-2.

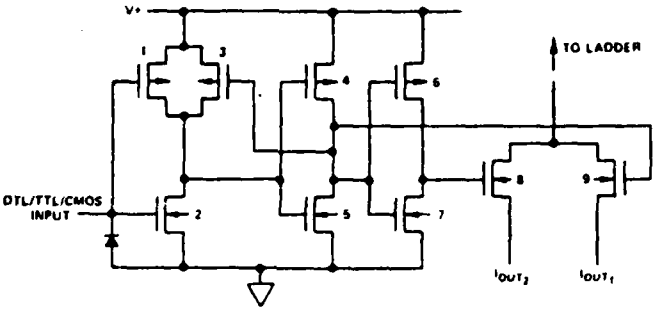


Figure 5-2. CMOS Switch Schematic

With the application of a DTL/TTL/CMOS compatible logic signal, two CMOS inverters assume the proper states to drive their respective output switches such that one is "ON" and the other "OFF". The end result is that the same ladder current is steered in either direction. A logic "high" input results in an Ioutl switch position and current flow.

Most applications of these R-2R ladder and switch networks involve an external operational amplifier configured as a current to voltage converter. The feedback resistor for this op amp is one of the deposited thin film resistors. Figure 5-3 shows how both devices are connected together to form a voltage output multiplying DAC. The digital input word determines the states of all of the bits from the MSB (Most Significant Bit) to the LSB (Least Significant Bit). All of the binary currents gated through logic "1" positioned switches flow through the feedback resistor to the op amp output. Therefore,

$$Eo = -Ioutl * Rfb$$

The current Ioutl is the product of the reference voltage and the digital binary fraction divided by the R-2R ladder input resistance.

$$Ioutl = D * Eref/Zin$$

where

$$D = B1*(1/2) + B2*(1/4) + B3*(1/8) + \ldots BN*(1/2\ expN)$$

B1 thru BN are 1 or 0.

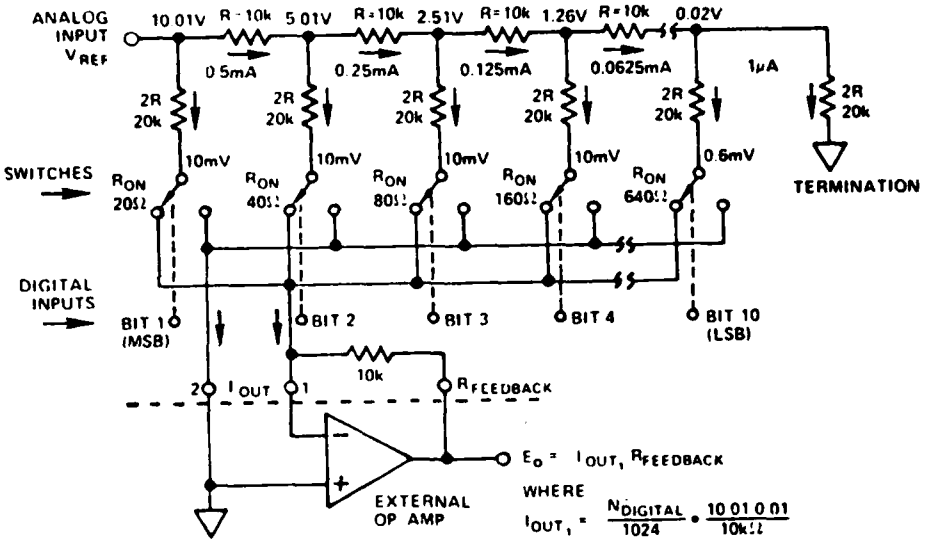


Figure 5-3. Typical Voltage Output MDAC Application

For the more common 2-quadrant multiplication application of an 8 bit device as shown in Figure 5-3, the relationship between digital input and analog output is as follows:

Digital Input	Analog Output
1111 1111	-VREF * (1 - 1/2 exp 8) = - VREF * (255/256)
....	
....	
1000 0001	-VREF * ((1/2) + (1/2 exp 8)) = VREF * (129/256)
1000 0000	-VREF * (1/2)
....	
....	
0000 0001	-VREF * (1/2 exp 8) = -VREF * (1/256)
0000 0000	0

This current mode DAC has an output impedance which varies with the input digital code word. Parasitic output capacitance interacting with this variable output impedance can result in poor closed loop response (either reduced bandwidth or ringing). A compensating capacitor across the output amplifier feedback resistor is recommended. Since the output impedance varies, the noise gain of the output op amp will result in a variable gain to noise and offsets. The op amp should therefore have low offset, low offset drift, and low noise. Also grounding techniques should be given careful consideration.

5.3 Test Development

A variety of devices were procured from three manufacturers as shown in Table 5.2.

Table 5.2. Device Types for Characterization.

Generic Type	Manufacturer	Quantity	Date Code
AD7523UD	Intersil	10*	7947
AD7523TD	Intersil	6*	7947
AD7520UD	Intersil	11*	7947
AD7520UD	Analog Devices	15	8006
AD7520UD	Analog Devices	10	8019
AD7521UD	Intersil	12*	7947
AD7521UD	Analog Devices	7*	8030
AD7541KD	Intersil	15*	7949
AD7541TD	Analog Devices	10	8038,8021
DAC1218	National	10*	8045

*Data was submitted with the devices.

Much of the test development for the CMOS MDAC characterization originated with the work done in characterizing the AD562 D/A converters. Many of the test techniques are similar.

CMOS MDAC Test Parameters

At a JC-41 meeting in August 1979 the manufacturers presented a proposed CMOS MDAC Specification. A list of parameters is shown in Table 5-3.

Table 5-3. Test Parameters for Characterization.

Item No	Symbol	Test Parameter
1	Icc	Supply Current
2	Iref	Reference Input Current
3	IIL	Digital Input Leakage Current (logic 0)
4	IIH	Digital Input Leakage Current (logic 1)
5	IZS	Zero Scale Current (IOUT1 at logic 0 input)
6	dIZS/dT	Zero Scale Current Drift
7	IZS'	Zero Scale Current (IOUT2 at logic 1 input)
8	+dVFS	Gain Error (Full Scale) with +10V Reference
9	-dVFS	Gain Error (Full Scale) with -10V Reference
10	dVFS/dT	Gain Error Drift
11	+PSS	Power Supply Sensitivity (+ 1V change)
12	-PSS	Power Supply Sensitivity (- 1V change)
13	LE	Linearity Error (End Point)
14	LE(BF)	Linearity Error (Best Fit)
15	MCE	Major Carry Error
16	FTE	Feedthrough Error
17	tSLH	Output Current Settling Time (low to high)
18	tSHL	Output Current Settling Time (high to low)
19	Co	Output Capacitance
20	en	Noise (broadband)

Test parameter items 1 through 15, except LE(BF) were setup to be measured on GEOS' S-3270 Automatic Tester. All of these parameters are static. The static test circuit is shown in Figure 5-4. This circuit is very similar to the one used in testing the AD562 D/A Converters. There were, however, several essential differences which had to be made. Since the CMOS multiplying D/A's use a variable reference, it was decided that data had to be taken for several reference voltage conditions. These conditions were chosen at + 10 V, - 10 V, and + 1.25 V. A Fluke 5100B was used to generate the different reference voltage levels. The 16 bit reference D/A converter was remotely located from the adapter through a ribbon cable so that it could be used with other test adapters. In order to maintain voltage accuracy at the adapter U6 error amplifier, the reference D/A output buffer U4 has its output to feedback connection made at the error amplifier output. Also a ground driver U2-U3 is used to force the DUT and adapter ground to be at the same potential as the external reference D/A. The IOUT1 current output of the DUT is converted to a voltage by means of op amp U5. Since a millivolt of op amp offset voltage at 10 volts full scale causes a 0.01% linearity error, it is important that this offset be trimmed out. In other words, Iout1 and Iout2 must go to virtual ground and output ground for proper operation. The offset adjustment of U5 is done with relays K1 and K4 energized. For any digital code word between zero scale and full scale, the test circuit and software are mechanized so that nearly equal and opposite voltages are generated by the reference D/A at the output of U4 and the DUT at the output of U5. The differences between these voltages is amplified by U6 with a gain setting of 100 V/V and appears at adapter output pin 21.

Since the reference D/A is accurate to 16 bits, it is assumed perfect and any error is charged against the DUT. The inverted voltage output of the DUT D/A at U5 is determined indirectly as follows:

$$EDUT = Eo/G - EREF\ D/A$$

$$EDUT = -Eo/100 - 10(N)/2 \exp B$$

where

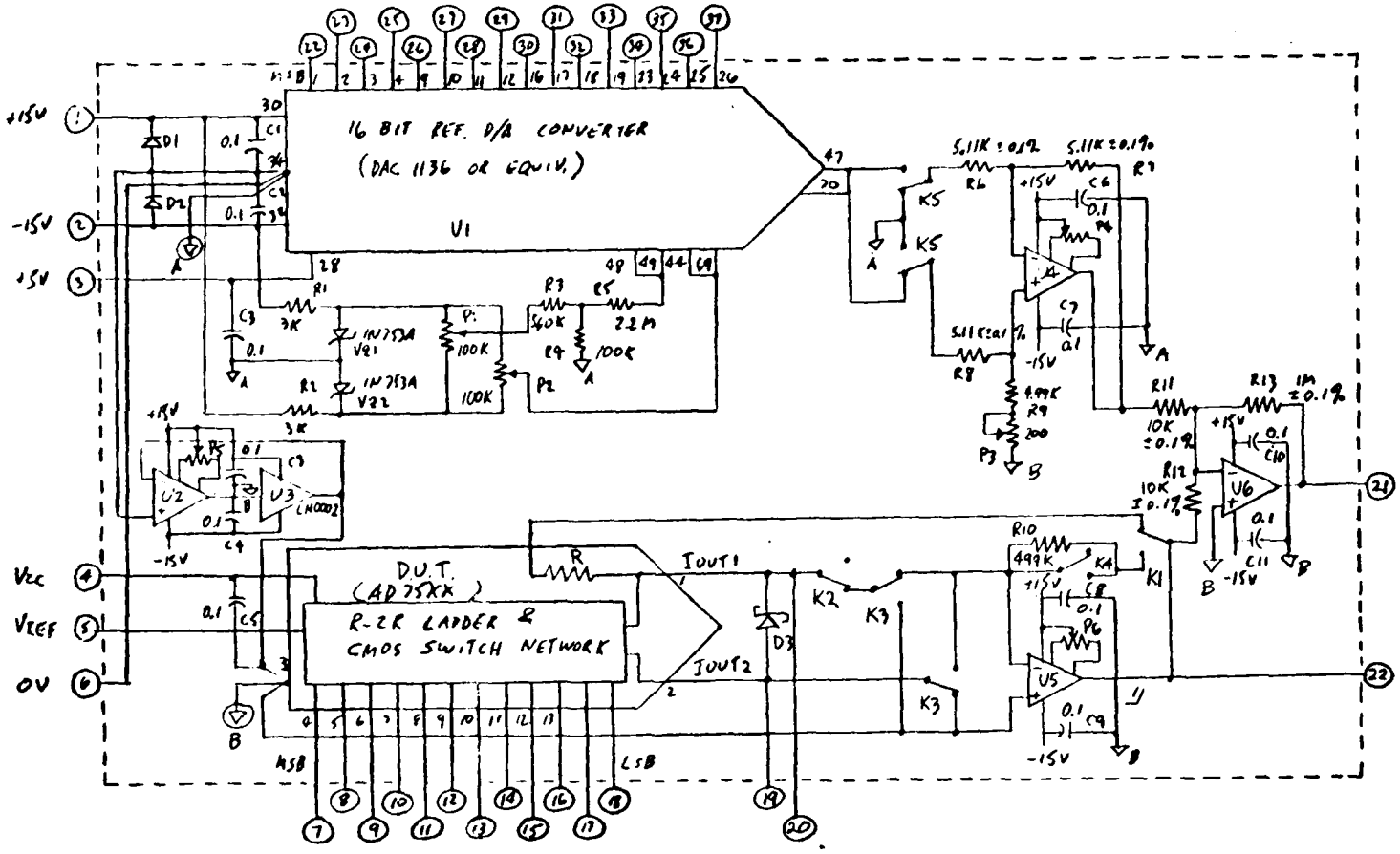
G = -100 V/V is the error amp gain

N = decimal equivalent of the input digital code word

B = number of bits

An inspection of the static test circuit shows that if the measured output voltage is positive, EDUT, although negative in polarity, has a greater magnitude than EREF D/A. Consequently, the DUT output has a positive scale error with respect to the Reference D/A.
The imaginary non-inverted value of the DUT D/A can then be written as

$$EDUT' = Eo/100 + 10(N)/2 \exp B$$



Notes: 1/ Op amp offset error ($V_{IO} + I_{IB} R_F$) adds to linearity error since I_{OUT1} and I_{OUT2} must go to 0V. For 10:1 measurement accuracy with a 12 bit DAC, acceptable op amps include the LF155, LF156 and OP-05 with V_{IO} (adj.) and the OP-07 without VIO (adj.).

2/ One millivolt of offset error on 10 VFS causes 0.01% linearity error.

Figure 5-4. Test circuit for static tests.

If a 12 bit MDAC at full scale had a measured adapter output Eo of 0.1 volts,

$$EDUT' = 0.1/100 + 10(4095)/4096$$

$$EDUT' = 0.001 + 9.99756\ V$$

$$EDUT' = 9.99856\ V$$

The full-scale error of the device in % can be determined from

$$+dVFS = [(-Eo(FS)/G1)/9.99756] \times 100\%$$

$$+dVFS = [(Eo(FS)/100)/9.99756] \times 100\%$$

$$+dVFS = 0.1\ Eo(FS)\ \%\ VFS$$

$$+dVFS = (0.1)(.1) = +\ 0.01\%\ VFS$$

In millivolts the full-scale error is + dVFS = 0.01% of 10,000 mV = 1 mV. The linearity error of the DUT output transfer characteristic from zero scale to full scale is perhaps the most important parameter to be measured. For characterization, GEOS's procedure has been to measure the adapter output error for all digital input codes. Thus for a 12 bit converter 4096 discrete measurements are required. Automatic calculations are then done to determine the deviation of each DUT output point from a straight line between the DUT's zero scale and full scale end points. Figure 5-5 shows the transfer characteristic of a hypothetical poor device compared to an ideal device.

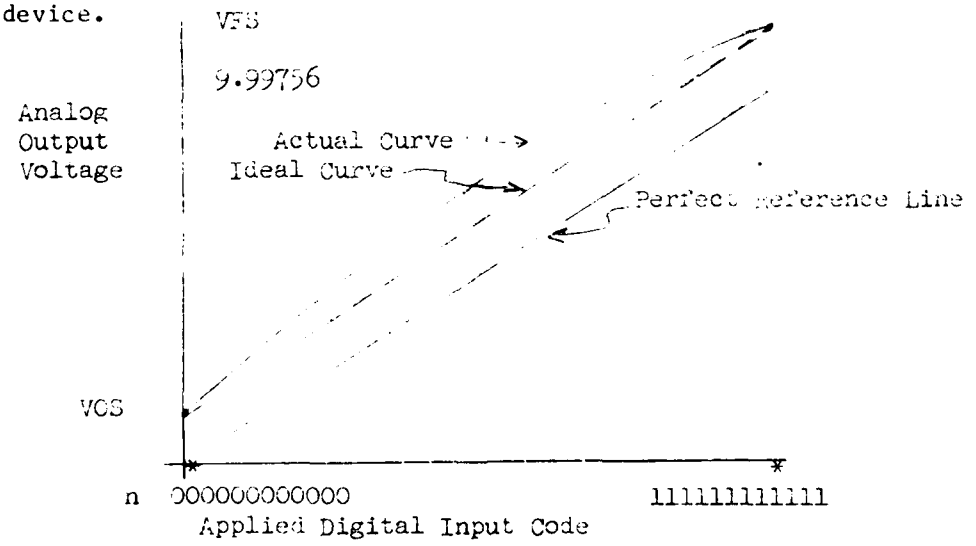


Figure 5-5. CMOS MDAC Transfer Characteristic.

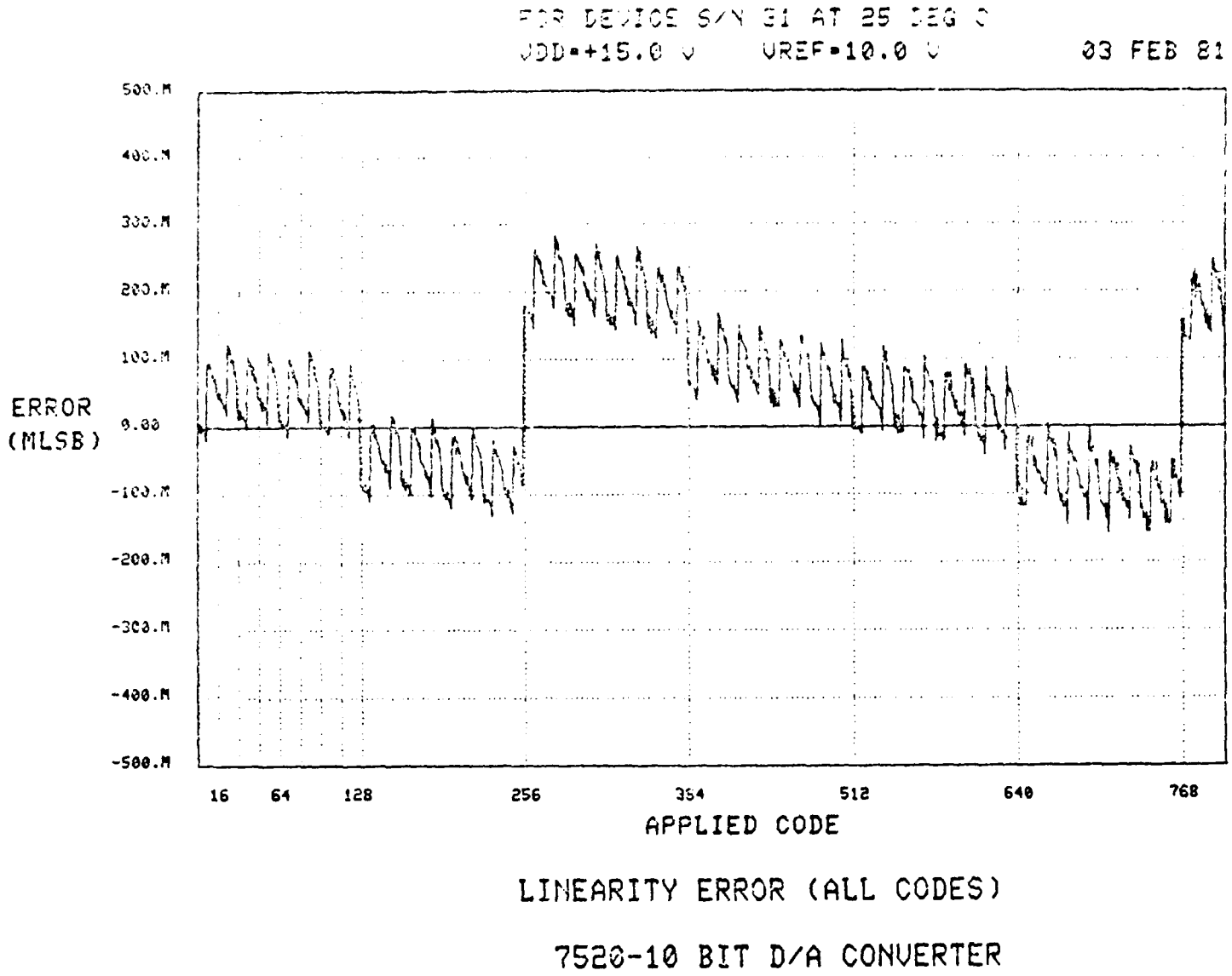


Figure 5-6. Automatic Linearity Plot

After the linearity error is determined for each point the data can be automatically plotted as shown in Figure 5-6, or it can be summarized by listing the individual bit errors and the worst case positive and worst case negative bit errors and associated address codes.

By comparison the remaining parameters to be measured with the static test circuit are determined quite easily. Relays K1 and K3 are energized to measure the zero scale currents at IOUT1 and IOUT2 using U5 as a current to voltage converter. Input reference current, which is a function of the 10V reference and the impedance of the R-2R ladder network is measured directly by energizing K2 with all bits high.

Feedthrough error, settling time and output capacitance were determined with separate test fixtures as shown in Figures 5-7, 5-8 and 5-9.

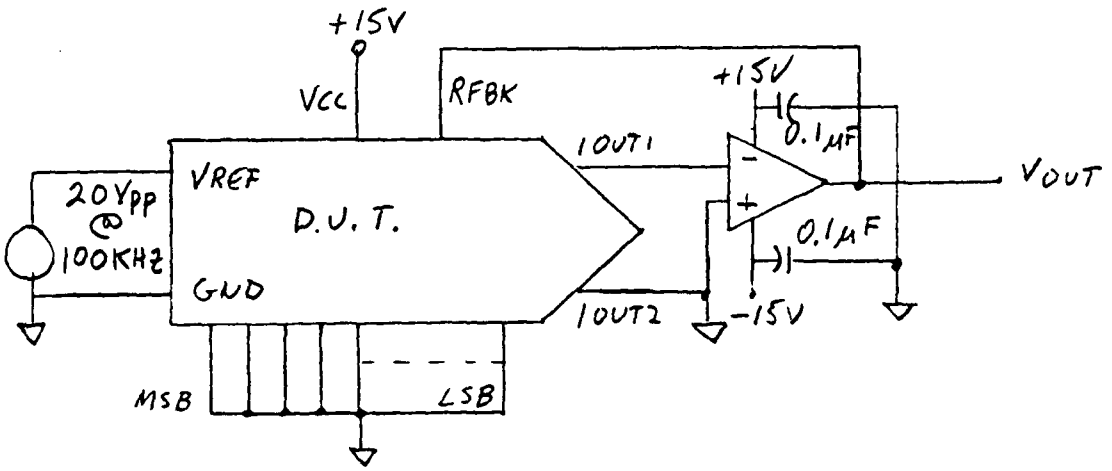


Figure 5-7. Feedthrough Error Test Circuit.

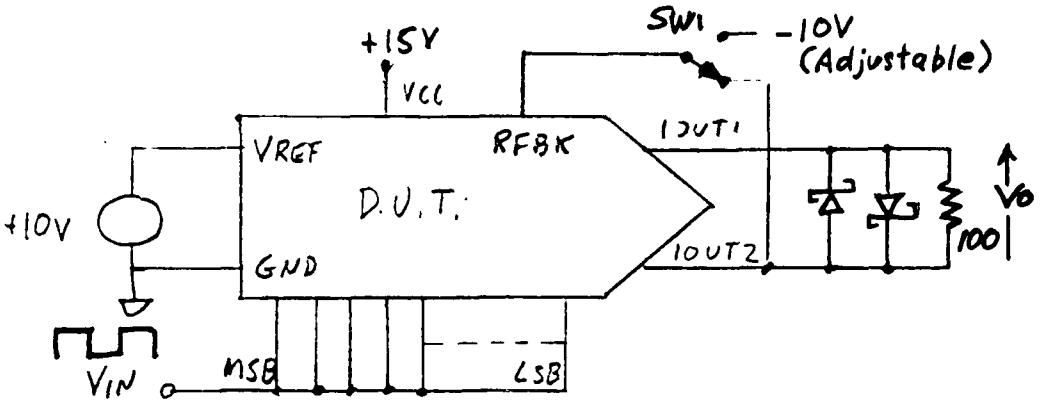
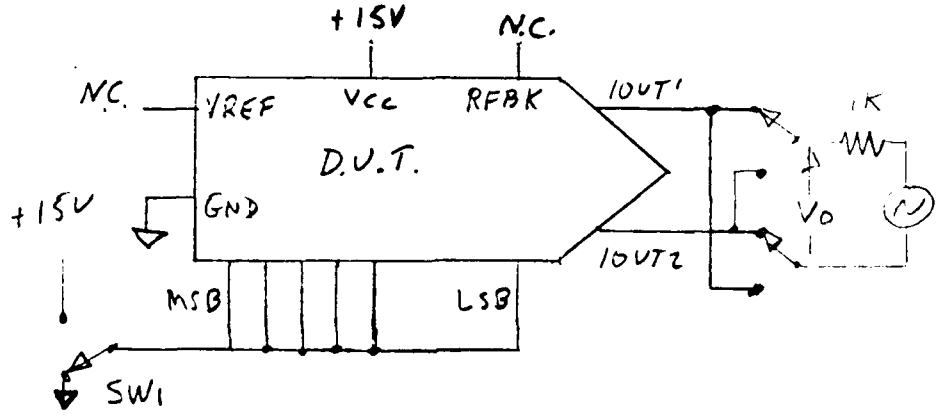


Figure 5-8. Setting Time Test Circuit.



Capacitance Test Circuit.

5.4 Test Results and Data

Characterization data was taken on twenty 10-bit devices from two vendors and fifteen 12-bit devices from three vendors. Each device was sequentially tested for all parameters at 25oC, -55oC and 125oC. The data was recorded in several different forms as follows:

1. A dedicated sheet for each device showing all parameters at all temperatures.
2. A comparison of the parameters of ten devices at one temperature on a sheet.
3. Parameter histograms of all devices at each temperature.
4. Plots of device bit linearity error vs applied digital input code.
5. Individual device histograms of bit linearity error vs frequency of occurrence.

The complete collection of data was published by GEOS in a handbook entitled:

Characterization Data for MIL-R-38510/127 CMOS Multiplying DA Converters (AD7520 & DAC 1020 Series)

Representative data sheets are shown in this report as follows:

Table 5-4	Typical Mfr. Code A Device Data Sheet
Table 5-5	Typical Mfr. Code B Device Data Sheet
Table 5-6	Typical Mfr. Code C Device Data Sheet
Table 5-7	Mfr. Code A Data (10 devices at 25oC)
Table 5-8	Mfr. Code B Data (10 devices at 25oC)
Table 5-9	Mfr. Code C Data (10 devices at 25oC)
Figure 5-10	Histogram of Gain Error (20 devices)
Figure 5-11	Linearity Error Distribution Histogram
Figure 5-12	Linearity Error vs Input Code Plot
Figure 5-13	Linearity Histogram at V_{REF} = + 10 V for S/N 2
Figure 5-14	Linearity Histogram at V_{REF} = - 10 V for S/N 2
Figure 5-15	Linearity Histogram at V_{REF} = 1.25 V for S/N 2
Figure 5-16	Linearity Plot at Vcc = +15 V
Figure 5-17	Linearity Plot at Vcc = +5 V

5-5 Discussion of Data

The characterization data in all forms was reviewed to see how well it compares to the original limits proposed by the JC-41 Committee. A discussion of this data on a parameter by parameter basis follows:

Power Supply Current (I_{cc})

The power supply current is much less than the indicated 100 uA limits when the digital inputs are at 0 V or V_{cc} respectively. GEOS' data for these conditions is wrong because in making the measurements, full-scale was set at the 100 uA recommended limit while the actual current was typically less than 1 uA. As a consequence the machine accuracy and offset error swamped out the reading to be measured. This data was retaken on the bench and, except for one device, all values were less than 1 uA. When the digital input levels were set at the 0.8 V to 2.4 V TTL compatible levels the supply current increased significantly, thus indicating more leakage in the OFF transistors of CMOS switches. At -55°C several vendor code B devices just exceeded the 2 mA maximum limit. GEOS recommends that the -55°C limit be raised to 2.5 mA.

Reference Current (IREF(+), IREF(-))

All of the data was between 0.8 and 1.3 mA compared to the 0.5 to 2 mA limits. This current reflects the value of the R-2R ladder network.

Digital Input Leakage Current (I_{IL}, I_{IH})

The individual device sheets were set up to indicate PASS or FAIL to summarize the results if any of the ten or twelve digital inputs had a failure No failures were recorded and the histograms indicated a spread between 0 and 43 nanoamperes.

Zero Scale Current (I_{ZS}, I_{ZS}')

Typical device data was much less than the recommended limits of +/- 200 nA. Except for one maverick device which measured -149.5 nA at 125°C, all other data was between -11 nA and 0. GEOS recommends that the limits be reduced to +/- 100 nA. It is believed that the single untypical value could be a measurement error because it does not agree with submitted vendor data.

Zero Scale Current Drift (dIZS/dT)

A review of the data indicates that limits of +/- 400 pA/°C would be reasonable. There was no JC-41 recommendation on this parameter.

Full Scale Error (+ dVFS, - dVFS)

The distribution of data between - 45.6 mV and 17.6 mV was well within the ± 100 mV recommended limits.

Full Scale Error Drift (dVFS/dT)

All of the data is within the ± 10 ppm VFS/V limits.

Power Supply Sensitivity (+ PSS, - PSS)

The distribution of data is very much tighter than the recommended limits of ± 100 ppm VFS/V. GEOS recommends that these limits be reduced to ± 50 ppm VFS/V.

Linearity Error (LE)

Linearity error is one parameter which cannot be negotiated. The linearity has to be within 1/2 LSB to meet the stated accuracy requirement. Most of the data is well within the ± 1/2 LSB limits. Figure 5-12 shows how the linearity for a typical device varies with its input code. Figures 5-13, 5-14 and 5-15 show the linearity histograms of one device (S/N 2) with V_{REF} = + 10 V, - 10 V and + 1.25 V respectively. Because of the apparent independence of reference voltage level the specification requirement to test at all three levels may be reduced to testing at + 10 V only.

Feedthrough Error (FTE)

All of the data for devices from vendors A and B were under 8.5 mVpp. These devices are within their 10 mVpp limit. Vendor Code C devices had feedthrough errors as high as 19 mVpp. These devices satisfy their 25 mVpp limit.

Output Current Settling Time (t_{SLH}, t_{SHL})

All devices had data values within the recommended 1 usec maximum limit.

Output Capacitance (CO)

All device data satisfies the JC-41 Committee's recommended limits.

5.6 Slash Sheet Development

The slash sheet, MIL-M-38510/127, was developed as a joint effort of GEOS and the JC-41 Committee/Subcommittee. The majority of the test parameters were established early in the slash sheet development in a JC-41 Subcommittee meeting. One major change has been the deletion of +5V as a recommended operating supply voltage. All-codes data taken on a 7520 device from vendor A showed excessive linearity errors and differential linearity errors, especially at +125°C. A comparison of one such sample of data taken at two supply voltages is shown in the Appendix, Table 5-16 and Table 5-17. GEOS' recommendation to limit operating voltage to +15 volts was adopted by the JC-41 committee.

A major goal of the characterization was to develop an abbreviated test for linearity. Initial all-codes testing of the 7520 linearity error showed that the abbreviated test used for the 562 12-bit D/A Converter specified in MIL-M-38510/121 was invalid for the 7520, since it did not find the worst case codes having maximum linearity error. The following approach to an abbreviated test was developed by GE and is proposed for the slash sheet:

1. Measure all combinations of the four MSB's with the lower order bits OFF.

2. Measure each of the lower order bits with the four MSB's OFF.

3. Determine the code word with the most positive predictable error based on the above tests, and measure that error. Repeat this measurement but with all lower order bits complemented one at a time.

4. Repeat the third group of tests above, but with the most negative predictable error codes.

This abbreviated test is done in Group A at three temperatures. An all-codes test at three temperatures is also required on a sample basis in the slash sheet.

This device is used as a multiplying DAC in many applications. Therefore, it is also necessary to test its ability to convert digital inputs with a negative reference voltage applied. GE has characterized the 7520 device at three refence voltage levels: +10V, - 10V, and + 1.25 V. Linearity errors are comparable at all three reference levels, although in many cases the error is slightly greater at minus ten volts than at plus ten volts. In order to guarantee the performance for both polarities, the abbreviated test is also required to be run at both plus and minus 10 volt levels, and at + 1.25 volts. This requirement will be further negotiated with the JC-41 committee.

Table I, Electrical Performance Characteristics, MIL-M-38510/127, is included in the following for reference.

5.7 Conclusions and Recommendations

The 7520 10-bit DAC (and the 7523 8-bit DAC which is manufactured using the 7520 chip) has been characterized and is judged suitable for use in military systems when procured via MIL-M 38510/127. Device manufacturers will review the characterization data and proposed slash sheet before the issuance of the final slash sheet.

The 7541 12-bit DACs have not yet been fully characterized at the time of writing of this report. That effort will be completed and integrated into the final released specification.

Table 5-4. Typical Mfr. Code A Device Data Sheet.

CMOS MULTIPLYING D/A CONVERTER DEVICE TYPE 7520 S/N 1 1 LSB= 5.775MV

PARAMETER	-55 DEG C LO-LIM	-55 DEG C DATA	-55 DEG C HI-LIM	25 DEG C LO-LIM	25 DEG C DATA	25 DEG C HI-LIM	+125 DEG C LO-LIM	+125 DEG C DATA	+125 DEG C HI-LIM	
ICC - ALL INPUTS AT 0.0V	0.00	-1.00	100.	0.00	-3.00	100.	0.00	-2.50	100.	UA
ICC - ALL INPUTS AT 1.0V	0.00	448. *	100.	0.00	560. *	100.	0.00	584. *	100.	UA
ICC - ALL INPUTS AT 0.8V	0.00	10.0M	2.00	0.00	5.00M	2.00	0.00	30.0M	2.00	MA
ICC - ALL INPUTS AT 2.4V	0.00	1.04	2.00	0.00	725.M	2.00	0.00	510.M	2.00	MA
IREF(+)-ALL INPUTS AT 15V	500.M	915.M	2.00	500.M	940.M	2.00	500.M	965.M	2.00	MA
IREF(-)-ALL INPUTS AT 15V	-2.00	-940.M	-500.M	-2.00	-960.M	-500.M	-2.00	-985.M	-500.M	MA
IIL - ALL INPUTS AT 0.0V	-1.00	PASSED	1.00	-1.00	PASSED	1.00	-1.00	PASSED	1.00	UA
IIL - ALL INPUTS AT 0.8V	-200.	PASSED	1.00	-200.	PASSED	1.00	-200.	PASSED	1.00	UA
IIH - ALL INPUTS AT 15.0V	-1.00	PASSED	1.00	-1.00	PASSED	1.00	-1.00	PASSED	1.00	UA
IIH - ALL INPUTS AT 2.4V	-1.00	PASSED	100.	-1.00	PASSED	100.	-1.00	PASSED	100.	UA
IZS - ALL INPUTS AT 0.0V	-200.	-3.00	200.	-200.	-2.50	200.	-200.	-6.50	200.	NA
IZS' - ALL INPUTS AT 2.4V	-200.	-2.50	200.	-200.	-2.00	200.	-200.	-6.50	200.	NA
dIZS/dT - INPUTS AT 0.0V	-50.0	6.25	50.0	0.00	0.00	0.00	-50.0	40.0	50.0	PA/oC
dIZS'/dT- INPUTS AT 2.4V	-50.0	6.25	50.0	0.00	0.00	0.00	-50.0	45.0	50.0	PA/oC
GAIN ERROR (VFS)	-100.	-16.5	100.	-100.	-11.5	100.	-100.	-4.55	100.	MV
GAIN ERROR (dVFS/dT)	-10.0	6.30	10.0	0.00	0.00	0.00	-10.0	-6.95	10.0	PPM
PSS - VCC=15V TO 16V	-100.	1.29	100.	-100.	-1.79	100.	-100.	-103.M	100.	PPM
PSS - VCC=15V TO 14V	-100.	-108.M	100.	-100.	527.M	100.	-100.	410.M	100.	PPM
BIT LINEARITY ERROR - MSB	-500.M	-4.48M	500.M	-500.M	-2.44M	500.M	-500.M	35.1M	500.M	LSB
BIT LINEARITY ERROR - B2	-500.M	124.M	500.M	-500.M	124.M	500.M	-500.M	145.M	500.M	LSB
BIT LINEARITY ERROR - B3	-500.M	84.3M	500.M	-500.M	90.3M	500.M	-500.M	94.4M	500.M	LSB
BIT LINEARITY ERROR - B4	-500.M	141.M	500.M	-500.M	141.M	500.M	-500.M	139.M	500.M	LSB
BIT LINEARITY ERROR - B5	-500.M	31.6M	500.M	-500.M	18.2M	500.M	-500.M	-4.60M	500.M	LSB
BIT LINEARITY ERROR - B6	-500.M	27.9M	500.M	-500.M	-6.58M	500.M	-500.M	-60.5M	500.M	LSB
BIT LINEARITY ERROR - B7	-500.M	11.8M	500.M	-500.M	34.4M	500.M	-500.M	58.3M	500.M	LSB
BIT LINEARITY ERROR - B8	-500.M	47.3M	500.M	-500.M	80.0M	500.M	-500.M	126.M	500.M	LSB
BIT LINEARITY ERROR - B9	-500.M	49.4M	500.M	-500.M	76.1M	500.M	-500.M	119.M	500.M	LSB
BIT LINEARITY ERROR - LSB	-500.M	37.2M	500.M	-500.M	56.5M	500.M	-500.M	84.1M	500.M	LSB
MAX(+) LINEARITY ERROR &	0.00	318.M	500.M	0.00	345.M	500.M	0.00	434.M	500.M	LSB
ASSOC ADDRESS (ALL CODES)	0.00	455.	0.00	0.00	455.	0.00	0.00	327.	0.00	DEC
MAX(+) LINEARITY ERROR &	0.00	284.M	500.M	0.00	334.M	500.M	0.00	422.M	500.M	LSB
ASSOC ADDRESS (ABBREV)	0.00	503.	0.00	0.00	463.	0.00	0.00	463.	0.00	DEC
MAX(-) LINEARITY ERROR &	-500.M	-115.M	0.00	-500.M	-183.M	0.00	-500.M	-262.M	0.00	LSB
ASSOC ADDRESS (ALL CODES)	0.00	956.	0.00	0.00	1.02K	0.00	0.00	952.	0.00	DEC
MAX(-) LINEARITY ERROR &	-500.M	-67.4M	0.00	-500.M	-167.M	0.00	-500.M	-262.M	0.00	LSB
ASSOC ADDRESS (ABBREV)	0.00	928.	0.00	0.00	944.	0.00	0.00	952.	0.00	DEC
MAX(+) LINEARITY ERROR &	0.00	307.M	500.M	0.00	344.M	500.M	0.00	437.M	500.M	LSB
ASSOC ADDRESS (VREF=-10V)	0.00	455.	0.00	0.00	455.	0.00	0.00	327.	0.00	DEC
MAX(-) LINEARITY ERROR &	-500.M	-83.7M	0.00	-500.M	-134.M	0.00	-500.M	-216.M	0.00	LSB
ASSOC ADDRESS (VREF=-10V)	0.00	956.	0.00	0.00	952.	0.00	0.00	952.	0.00	DEC
MAX(+) LINEARITY ERROR &	0.00	214.M	500.M	0.00	264.M	500.M	0.00	358.M	500.M	LSB
ASSOC ADDR (VREF=+1.25V)	0.00	327.	0.00	0.00	327.	0.00	0.00	463.	0.00	DEC
MAX(-) LINEARITY ERROR &	-500.M	-173.M	0.00	-500.M	-204.M	0.00	-500.M	-293.M	0.00	LSB
ASSOC ADDR (VREF=+1.25V)	0.00	668.	0.00	0.00	668.	0.00	0.00	762.	0.00	DEC

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 5-5. Typical Mfr. Code B Device Data Sheet.

CMOS MULTIPLYING D/A CONVERTER DEVICE TYPE 7520 S/N 31 1 LSB= 9.775MV

PARAMETER	-55 DEG C LO-LIM	-55 DEG C DATA	-55 DEG C HI-LIM	25 DEG C LO-LIM	25 DEG C DATA	25 DEG C HI-LIM	+125 DEG C LO-LIM	+125 DEG C DATA	+125 DEG C HI-LIM	
ICC - ALL INPUTS AT 0.0V	0.00	-1.00	100.	0.00	-1.50	100.	0.00	-3.00	100.	UA
ICC - ALL INPUTS AT 15.0V	0.00	472. *	100.	0.00	704. *	100.	0.00	748. *	100.	UA
ICC - ALL INPUTS AT 0.8V	0.00	20.0M	2.00	0.00	170.M	2.00	0.00	400.M	2.00	MA
ICC - ALL INPUTS AT 2.4V	0.00	2.06 *	2.00	0.00	1.35	2.00	0.00	985.M	2.00	MA
IREF(+)-ALL INPUTS AT 15V	500.M	1.26	2.00	500.M	1.27	2.00	500.M	1.31	2.00	MA
IREF(-)-ALL INPUTS AT 15V	-2.00	-1.27	-500.M	-2.00	-1.30	-500.M	-2.00	-1.33	-500.M	MA
IIL - ALL INPUTS AT 0.0V	-1.00	PASSED	1.00	-1.00	PASSED	1.00	-1.00	PASSED	1.00	UA
IIL - ALL INPUTS AT 0.8V	-200.	PASSED	1.00	-200.	PASSED	1.00	-200.	PASSED	1.00	UA
IIH - ALL INPUTS AT 15.0V	-1.00	PASSED	1.00	-1.00	PASSED	1.00	-1.00	PASSED	1.00	UA
IIH - ALL INPUTS AT 2.4V	-1.00	PASSED	100.	-1.00	PASSED	100.	-1.00	PASSED	100.	UA
IZS - ALL INPUTS AT 0.0V	-200.	-2.00	200.	-200.	-2.00	200.	-200.	-14.0	200.	NA
IZS' - ALL INPUTS AT 2.4V	-200.	-3.00	200.	-200.	0.00	200.	-200.	-10.0	200.	NA
dIZS/dT - INPUTS AT 0.0V	-50.0	0.00	50.0	0.00	0.00	0.00	-50.0	120. *	50.0	PA/oC
dIZS'/dT- INPUTS AT 2.4V	-50.0	37.5	50.0	0.00	0.00	0.00	-50.0	100. *	50.0	PA/oC
GAIN ERROR (VFS)	-100.	-37.7	100.	-100.	-32.2	100.	-100.	-24.3	100.	MV
GAIN ERROR (dVFS/dT)	-10.0	6.87	10.0	0.00	0.00	0.00	-10.0	-7.90	10.0	PPM
PSS - VCC=15V TO 16V	-100.	317.M	100.	-100.	155.M	100.	-100.	1.00	100.	PPM
PSS - VCC=15V TO 14V	-100.	1.27	100.	-100.	-311.M	100.	-100.	-385.M	100.	PPM
BIT LINEARITY ERROR - MSB	-500.M	4.57M	500.M	-500.M	6.23M	500.M	-500.M	925.U	500.M	LSB
BIT LINEARITY ERROR - B2	-500.M	186.M	500.M	-500.M	189.M	500.M	-500.M	163.M	500.M	LSB
BIT LINEARITY ERROR - B3	-500.M	-84.5M	500.M	-500.M	-90.0M	500.M	-500.M	-94.8M	500.M	LSB
BIT LINEARITY ERROR - B4	-500.M	12.7M	500.M	-500.M	2.85M	500.M	-500.M	-6.69M	500.M	LSB
BIT LINEARITY ERROR - B5	-500.M	21.3M	500.M	-500.M	16.8M	500.M	-500.M	4.29M	500.M	LSB
BIT LINEARITY ERROR - B6	-500.M	29.4M	500.M	-500.M	43.9M	500.M	-500.M	55.4M	500.M	LSB
BIT LINEARITY ERROR - B7	-500.M	70.9M	500.M	-500.M	88.4M	500.M	-500.M	114.M	500.M	LSB
BIT LINEARITY ERROR - B8	-500.M	-11.3M	500.M	-500.M	-1.48M	500.M	-500.M	7.72M	500.M	LSB
BIT LINEARITY ERROR - B9	-500.M	-2.36M	500.M	-500.M	2.79M	500.M	-500.M	5.83M	500.M	LSB
BIT LINEARITY ERROR - LSB	-500.M	886.U	500.M	-500.M	-3.05M	500.M	-500.M	-7.51M	500.M	LSB
MAX(+) LINEARITY ERROR &	0.00	265.M	500.M	0.00	277.M	500.M	0.00	311.M	500.M	LSB
ASSOC ADDRESS (ALL CODES)	0.00	280.	0.00	0.00	280.	0.00	0.00	280.	0.00	DEC
MAX(+) LINEARITY ERROR &	0.00	256.M	500.M	0.00	270.M	500.M	0.00	280.M	500.M	LSB
ASSOC ADDRESS (ABBREV)	0.00	312.	0.00	0.00	282.	0.00	0.00	286.	0.00	DEC
MAX(-) LINEARITY ERROR &	-500.M	-191.M	0.00	-500.M	-205.M	0.00	-500.M	-243.M	0.00	LSB
ASSOC ADDRESS (ALL CODES)	0.00	759.	0.00	0.00	743.	0.00	0.00	743.	0.00	DEC
MAX(-) LINEARITY ERROR &	-500.M	-171.M	0.00	-500.M	-199.M	0.00	-500.M	-228.M	0.00	LSB
ASSOC ADDRESS (ABBREV)	0.00	726.	0.00	0.00	741.	0.00	0.00	737.	0.00	DEC
MAX(+) LINEARITY ERROR &	0.00	239.M	500.M	0.00	249.M	500.M	0.00	317.M	500.M	LSB
ASSOC ADDRESS (VREF=-10V)	0.00	776.	0.00	0.00	280.	0.00	0.00	280.	0.00	DEC
MAX(-) LINEARITY ERROR &	-500.M	-165.M	0.00	-500.M	-190.M	0.00	-500.M	-192.M	0.00	LSB
ASSOC ADDRESS (VREF=-10V)	0.00	727.	0.00	0.00	743.	0.00	0.00	741.	0.00	DEC
MAX(+) LINEARITY ERROR &	0.00	252.M	500.M	0.00	243.M	500.M	0.00	275.M	500.M	LSB
ASSOC ADDR (VREF=+1.25V)	0.00	281.	0.00	0.00	280.	0.00	0.00	776.	0.00	DEC
MAX(-) LINEARITY ERROR &	-500.M	-180.M	0.00	-500.M	-185.M	0.00	-500.M	-204.M	0.00	LSB
ASSOC ADDR (VREF=+1.25V)	0.00	759.	0.00	0.00	741.	0.00	0.00	229.	0.00	DEC

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 5-6. Typical Mfr. Code C Device Data Sheet.

CMOS MULTIPLYING D/A CONVERTER DEVICE TYPE 1218 S/N 9 1 LSB= 2.442MV

PARAMETER	-55 DEG C LO-LIM	-55 DEG C DATA	-55 DEG C HI-LIM	25 DEG C LO-LIM	25 DEG C DATA	25 DEG C HI-LIM	+125 DEG C LO-LIM	+125 DEG C DATA	+125 DEG C HI-LIM	
ICC - ALL INPUTS AT 0.0V	0.00	1.69	2.00	0.00	1.25	2.00	0.00	955.M	2.00	UA
ICC - ALL INPUTS AT 15.0V	0.00	730.M	2.00	0.00	740.M	2.00	0.00	655.M	2.00	UA
ICC - ALL INPUTS AT 0.8V	0.00	1.70	2.00	0.00	1.20	2.00	0.00	980.M	2.00	MA
ICC - ALL INPUTS AT 2.4V	0.00	625.M	2.00	0.00	440.M	2.00	0.00	295.M	2.00	MA
IREF(+)-ALL INPUTS AT 15V	500.M	625.M	2.00	500.M	620.M	2.00	500.M	630.M	2.00	MA
IREF(-)-ALL INPUTS AT 15V	-2.00	-625.M	-500.M	-2.00	-635.M	-500.M	-2.00	-640.M	-500.M	MA
IIL - ALL INPUTS AT 0.0V	-200.	PASSED	1.00	-200.	PASSED	1.00	-200.	PASSED	1.00	UA
IIL - ALL INPUTS AT 0.8V	-200.	PASSED	1.00	-200.	PASSED	1.00	-200.	PASSED	1.00	UA
IIH - ALL INPUTS AT 15.0V	-200.	PASSED	1.00	-200.	PASSED	1.00	-200.	FAILED	1.00	UA
IIH - ALL INPUTS AT 2.4V	-1.00	FAILED	100.	-1.00	PASSED	100.	-1.00	PASSED	100.	UA
IZS - ALL INPUTS AT 0.0V	-200.	-160.	200.	-200.	-160.	200.	-200.	-4.38K *	200.	NA
IZS' - ALL INPUTS AT 2.4V	-200.	-130.	200.	-200.	-135.	200.	-200.	-195.	200.	NA
dIZS/dT - INPUTS AT 0.0V	-50.0	0.00	50.0	0.00	0.00	0.00	-50.0	42.2K *	50.0	PA/oC
dIZS'/dT- INPUTS AT 2.4V	-50.0	-62.5 *	50.0	0.00	0.00	0.00	-50.0	600. *	50.0	PA/oC
GAIN ERROR (VFS)	-100.	-907.M	100.	-100.	-1.97	100.	-100.	-3.66	100.	MV
GAIN ERROR (dVFS/dT)	-10.0	-1.32	10.0	0.00	0.00	0.00	-10.0	1.69	10.0	PPM
PSS - VCC=15V TO 16V	-100.	300.M	100.	-100.	300.M	100.	-100.	-4.00	100.	PPM
PSS - VCC=15V TO 14V	-100.	950.M	100.	-100.	-1.05	100.	-100.	2.00	100.	PPM
BIT LINEARITY ERROR - MSB	-500.M	41.5M	500.M	-500.M	50.3M	500.M	-500.M	674.M *	500.M	LSB
BIT LINEARITY ERROR - B2	-500.M	88.9M	500.M	-500.M	85.0M	500.M	-500.M	128.M	500.M	LSB
BIT LINEARITY ERROR - B3	-500.M	3.67M	500.M	-500.M	-3.00M	500.M	-500.M	208.M	500.M	LSB
BIT LINEARITY ERROR - B4	-500.M	-211.M	500.M	-500.M	-206.M	500.M	-500.M	-52.5M	500.M	LSB
BIT LINEARITY ERROR - B5	-500.M	70.1M	500.M	-500.M	75.3M	500.M	-500.M	177.M	500.M	LSB
BIT LINEARITY ERROR - B6	-500.M	114.M	500.M	-500.M	121.M	500.M	-500.M	169.M	500.M	LSB
BIT LINEARITY ERROR - B7	-500.M	33.3M	500.M	-500.M	33.4M	500.M	-500.M	59.0M	500.M	LSB
BIT LINEARITY ERROR - B8	-500.M	-29.5M	500.M	-500.M	-24.8M	500.M	-500.M	-19.7M	500.M	LSB
BIT LINEARITY ERROR - B9	-500.M	34.0M	500.M	-500.M	13.5M	500.M	-500.M	-7.78M	500.M	LSB
BIT LINEARITY ERROR - B10	-500.M	33.8M	500.M	-500.M	28.1M	500.M	-500.M	27.9M	500.M	LSB
BIT LINEARITY ERROR - B11	-500.M	43.2M	500.M	-500.M	40.4M	500.M	-500.M	47.7M	500.M	LSB
BIT LINEARITY ERROR - LSB	-500.M	50.5M	500.M	-500.M	43.8M	500.M	-500.M	53.6M	500.M	LSB
MAX(+) LINEARITY ERROR &	0.00	308.M	500.M	0.00	328.M	500.M	0.00	1.38 *	500.M	LSB
ASSOC ADDRESS (ALL CODES)	0.00	3.81K	0.00	0.00	3.30K	0.00	0.00	3.27K	0.00	DEC
MAX(+) LINEARITY ERROR &	0.00	298.M	500.M	0.00	328.M	500.M	0.00	1.33 *	500.M	LSB
ASSOC ADDRESS (ABBREV)	0.00	3.31K	0.00	0.00	3.30K	0.00	0.00	3.81K	0.00	DEC
MAX(-) LINEARITY ERROR &	-500.M	-284.M	0.00	-500.M	-257.M	0.00	-500.M	-80.7M	0.00	LSB
ASSOC ADDRESS (ALL CODES)	0.00	2.84K	0.00	0.00	796.	0.00	0.00	264.	0.00	DEC
MAX(-) LINEARITY ERROR &	-500.M	-272.M	0.00	-500.M	-254.M	0.00	-500.M	-78.3M	0.00	LSB
ASSOC ADDRESS (ABBREV)	0.00	784.	0.00	0.00	792.	0.00	0.00	792.	0.00	DEC
MAX(+) LINEARITY ERROR &	0.00	235.M	500.M	0.00	209.M	500.M	0.00	4.01 *	500.M	LSB
ASSOC ADDRESS (VREF=-10V)	0.00	272.	0.00	0.00	280.	0.00	0.00	511.	0.00	DEC
MAX(-) LINEARITY ERROR &	-500.M	-437.M	0.00	-500.M	-507.M *	0.00	-500.M	-3.71 *	0.00	LSB
ASSOC ADDRESS (VREF=-10V)	0.00	3.82K	0.00	0.00	3.78K	0.00	0.00	3.59K	0.00	DEC
MAX(+) LINEARITY ERROR &	0.00	248.M	500.M	0.00	231.M	500.M	0.00	1.99 *	500.M	LSB
ASSOC ADDR (VREF=+1.25V)	0.00	111.	0.00	0.00	71.0	0.00	0.00	2.82K	0.00	DEC
MAX(-) LINEARITY ERROR &	-500.M	-876.M *	0.00	-500.M	-516.M *	0.00	-500.M	-724.M *	0.00	LSB
ASSOC ADDR (VREF=+1.25V)	0.00	2.96K	0.00	0.00	2.83K	0.00	0.00	1.29K	0.00	DEC

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 5-7. Mfr. Code A Data @ 25°C

CMOS MULTIPLYING D/A CONVERTER DEVICE TYPE 7520 VREF = +10. EXCEPT WHERE SPECIFIED 1 LSB= 9.7754V

29 JAN 80 10:22:23 VDD = 15.0 VOLTS TEMPERATURE = +25 DEGREES C

PARAMETER	LO-LIM	S/N 1	S/N 2	S/N 3	S/N 4	S/N 5	S/N 6	S/N 7	S/N 8	S/N 9	S/N10	HI-LIM	UNITS
ICC - ALL INPUTS AT 0.0V	0.00	-3.00	-2.00	-4.50	-1.00	-6.50	-500.M	-2.00	-4.00	2.00	-500.M	100.	UA
ICC - ALL INPUTS AT 15.0V	0.00	560. *	416. *	515. *	449. *	472. *	528. *	466. *	679. *	457. *	428. *	100.	UA
ICC - ALL INPUTS AT 0.8V	0.00	5.00M	50.0M	35.0M	20.0M	5.00M	40.0M	0.00	5.00M	0.00	20.0M	2.00	MA
ICC - ALL INPUTS AT 2.4V	0.00	725.M	720.M	640.M	675.M	670.M	665.M	705.M	605.M	635.M	755.M	2.00	MA
IREF(+)-ALL INPUTS AT 15V	500.M	940.M	865.M	1.06	850.M	885.M	1.05	825.M	1.10	865.M	845.M	2.00	MA
IREF(-)-ALL INPUTS AT 15V	-2.00	-960.M	-895.M	-1.09	-875.M	-905.M	-1.09	-850.M	-1.12	-890.M	-860.M	-500.M	MA
IIL - ALL INPUTS AT 0.0V	-1.00	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	1.00	UA
IIL - ALL INPUTS AT 0.8V	-200.	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	1.00	UA
IIH - ALL INPUTS AT 15.0V	-1.00	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	1.00	UA
IIH - ALL INPUTS AT 2.4V	-1.00	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	100.	UA
IZS - ALL INPUTS AT 0.0V	-200.	-2.50	-2.50	-2.50	-3.00	-2.50	-5.00	-3.00	-5.50	-4.50	-4.50	200.	NA
IZS' - ALL INPUTS AT 2.4V	-200.	-2.00	-2.50	-1.50	-2.00	-2.50	-2.00	-1.50	-2.50	-2.00	0.00	200.	NA
dIZS/dT - INPUTS AT 0.0V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA/oC
dIZS'/dT- INPUTS AT 2.4V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA/oC
GAIN ERROR (VFS)	-100.	-11.5	17.6	15.3	-1.12	1.42	5.80	4.03	-8.22	-3.52	8.90	100.	MV
GAIN ERROR (dVFS/dT)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PPM
PSS - VCC=15V TO 16V	-100.	-1.79	-684.M	279.M	116.M	-334.M	93.6M	0.00	180.M	-457.M	1.18	100.	PPM
PSS - VCC=15V TO 14V	-100.	527.M	-1.03	1.77	1.39	-1.56	-1.03	-2.15	1.26	0.00	1.06	100.	PPM
BIT LINEARITY ERROR - MSB	-500.M	-2.44M	372.M	127.M	4.83M	2.73M	116.M	-142.M	-176.M	-157.M	-68.3M	500.M	LSB
BIT LINEARITY ERROR - B2	-500.M	124.M	39.9M	80.2M	47.5M	-220.M	-67.5M	38.7M	165.M	40.4M	182.M	500.M	LSB
BIT LINEARITY ERROR - B3	-500.M	90.3M	-73.6M	87.1M	111.M	213.M	110.M	47.5M	163.M	189.M	34.7M	500.M	LSB
BIT LINEARITY ERROR - B4	-500.M	141.M	72.8M	136.M	136.M	242.M	175.M	225.M	216.M	212.M	116.M	500.M	LSB
BIT LINEARITY ERROR - B5	-500.M	18.2M	-41.2M	12.4M	31.9M	48.4M	61.3M	78.1M	34.2M	20.8M	-6.43M	500.M	LSB
BIT LINEARITY ERROR - B6	-500.M	-6.58M	-76.8M	-4.80M	6.72M	22.6M	6.65M	25.6M	-38.7M	-18.9M	-54.2M	500.M	LSB
BIT LINEARITY ERROR - B7	-500.M	34.4M	62.7M	34.1M	31.7M	55.7M	63.0M	45.0M	106.M	80.3M	65.7M	500.M	LSB
BIT LINEARITY ERROR - B8	-500.M	80.0M	97.2M	92.5M	79.2M	80.6M	103.M	81.3M	127.M	113.M	96.3M	500.M	LSB
BIT LINEARITY ERROR - B9	-500.M	76.1M	91.5M	91.8M	76.3M	77.6M	97.4M	77.2M	112.M	61.2M	84.1M	500.M	LSB
BIT LINEARITY ERROR - LSB	-500.M	56.5M	59.7M	68.3M	55.7M	54.3M	71.2M	59.6M	76.9M	49.3M	61.2M	500.M	LSB
MAX(+) LINEARITY ERROR &	0.00	345.M	574.M*	365.M	330.M	547.M*	408.M	403.M	614.M*	525.M*	438.M	500.M	LSB
ASSOC ADDRESS (ALL CODES)	----	455	591	583	199	207	591	103	463	207	335	----	DEC
MAX(+) LINEARITY ERROR &	0.00	334.M	81.8M	351.M	191.M	537.M*	388.M	388.M	556.M*	525.M*	286.M	500.M	LSB
ASSOC ADDRESS (ABBREV)	----	463	463	591	623	239	239	239	207	207	207	----	DEC
MAX(-) LINEARITY ERROR &	-500.M	-183.M	-300.M	-186.M	-191.M	-350.M	-241.M	-296.M	-325.M	-323.M	-248.M	0.00	LSB
ASSOC ADDRESS (ALL CODES)	----	1016	432	952	952	784	952	920	944	816	944	----	DEC
MAX(-) LINEARITY ERROR &	-500.M	-167.M	-157.M	-135.M	-122.M	-350.M	-122.M	-289.M	-325.M	-287.M	-248.M	0.00	LSB
ASSOC ADDRESS (ABBREV)	----	944	944	944	912	784	784	912	944	944	944	----	DEC
MAX(+) LINEARITY ERROR &	0.00	344.M	573.M*	392.M	320.M	533.M*	424.M	394.M	600.M*	501.M*	434.M	500.M	LSB
ASSOC ADDRESS (VREF=-10V)	----	455	591	583	199	207	583	359	463	207	335	----	DEC
MAX(-) LINEARITY ERROR &	-500.M	-134.M	-289.M	-107.M	-111.M	-300.M	-173.M	-231.M	-264.M	-272.M	-213.M	0.00	LSB
ASSOC ADDRESS (VREF=-10V)	----	952	440	952	952	816	952	952	944	816	688	----	DEC
MAX(+) LINEARITY ERROR &	0.00	264.M	491.M	273.M	299.M	516.M*	342.M	389.M	504.M*	492.M	382.M	500.M	LSB
ASSOC ADDR (VREF=+1.25V)	----	327	527	71	199	207	79	103	463	207	335	----	DEC
MAX(-) LINEARITY ERROR &	-500.M	-204.M	-399.M	-154.M	-194.M	-415.M	-222.M	-293.M	-435.M	-407.M	-283.M	0.00	LSB
ASSOC ADDR (VREF=+1.25V)	----	568	496	952	816	816	816	920	560	816	688	----	DEC

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 5-8. Mfr. Code B Data @ 25°C.

CMOS MULTIPLYING D/A CONVERTER DEVICE TYPE 7520 VREF = +10V EXCEPT WHERE SPECIFIED 1 LSB= 9.775MV

29 JAN 80 10:23:42 VDD = 15.0 VOLTS TEMPERATURE = +25 DEGREES C

PARAMETER	LO-LIM	S/N31	S/N32	S/N33	S/N34	S/N35	S/N36	S/N37	S/N38	S/N39	S/N40	HI-LIM	UNITS
ICC - ALL INPUTS AT 0.0V	0.00	-1.50	-4.50	2.00	-2.00	-3.50	-1.00	-3.50	-6.50	-1.00	-3.00	100.	UA
ICC - ALL INPUTS AT 15.0V	0.00	704. %	612. %	680. %	652. %	677. %	508. %	576. %	603. %	-500.M	608. %	100.	UA
ICC - ALL INPUTS AT 0.8V	0.00	170.M	115.M	75.0M	160.M	335.M	80.0M	140.M	410.M	25.0M	470.M	2.00	MA
ICC - ALL INPUTS AT 2.4V	0.00	1.35	1.35	1.32	1.30	1.36	1.36	1.30	1.28	1.38	1.31	2.00	MA
IREF(+)-ALL INPUTS AT 15V	500.M	1.27	1.24	1.27	1.20	1.23	950.M	1.04	1.22	1.08	1.29	2.00	MA
IREF(-)-ALL INPUTS AT 15V	-2.00	-1.30	-1.26	-1.30	-1.23	-1.26	-975.M	-1.06	-1.24	-1.10	-1.32	-500.M	MA
IIL - ALL INPUTS AT 0.0V	-1.00	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	1.00	UA
IIL - ALL INPUTS AT 0.8V	-200.	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	1.00	UA
IIH - ALL INPUTS AT 15.0V	-1.00	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	1.00	UA
IIH - ALL INPUTS AT 2.4V	-1.00	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS	100.	UA
IZS - ALL INPUTS AT 0.0V	-200.	-2.00	-3.00	-3.50	-4.50	-3.50	-3.50	-6.00	-3.00	-3.50	-3.00	200.	NA
IZS' - ALL INPUTS AT 2.4V	-200.	0.00	0.00	0.00	-2.00	-2.50	0.00	-1.00	-2.50	-2.50	-2.50	200.	NA
dIZS/dT - INPUTS AT 0.0V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA/oC
dIZS'/dT- INPUTS AT 2.4V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA/oC
GAIN ERROR (VFS)	-100.	-32.2	-34.0	-28.6	-37.0	-32.3	-41.7	-45.6	-28.4	-40.2	-29.4	100.	MV
GAIN ERROR (dVFS/dT)	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PPM
PSS - VCC=15V TO 16V	-100.	155.M	321.M	-859.M	82.2M	644.M	208.M	191.M	978.M	460.M	-1.23	100.	PPM
PSS - VCC=15V TO 14V	-100.	-311.M	723.M	390.M	-1.07	805.M	936.M	1.05	162.M	1.20	385.M	100.	PPM
BIT LINEARITY ERROR - MSB	-500.M	6.23M	280.M	-288.M	121.M	16.5M	-189.M	362.M	-74.5M	-277.M	263.M	500.M	LSB
BIT LINEARITY ERROR - B2	-500.M	189.M	187.M	7.74M	246.M	322.M	280.M	136.M	318.M	27.7M	168.M	500.M	LSB
BIT LINEARITY ERROR - B3	-500.M	-90.0M	-10.7M	72.8M	-103.M	-42.4M	-32.9M	-168.M	-88.6M	-32.8M	-111.M	500.M	LSB
BIT LINEARITY ERROR - B4	-500.M	2.85M	-122.M	121.M	-32.5M	-37.2M	52.6M	-100.M	-15.5M	195.M	-62.2M	500.M	LSB
BIT LINEARITY ERROR - B5	-500.M	16.8M	-71.9M	62.9M	-37.3M	-38.2M	37.6M	-29.8M	-26.1M	24.3M	-31.6M	500.M	LSB
BIT LINEARITY ERROR - B6	-500.M	43.9M	-12.8M	116.M	5.53M	14.6M	22.6M	7.12M	52.6M	141.M	4.52M	500.M	LSB
BIT LINEARITY ERROR - B7	-500.M	88.4M	67.1M	121.M	75.2M	64.6M	77.9M	56.1M	79.6M	132.M	71.6M	500.M	LSB
BIT LINEARITY ERROR - B8	-500.M	-1.48M	-32.9M	-296.U	-16.1M	-27.9M	-29.9M	-27.6M	-13.7M	5.60M	-23.4M	500.M	LSB
BIT LINEARITY ERROR - B9	-500.M	2.79M	-27.2M	10.4M	-10.0M	-13.6M	-26.5M	-23.8M	399.U	12.4M	-15.3M	500.M	LSB
BIT LINEARITY ERROR - LSB	-500.M	-3.05M	-12.6M	8.93M	-6.87M	-12.1M	4.36M	-10.1M	366.U	15.6M	-17.2M	500.M	LSB
MAX(+) LINEARITY ERROR &	0.00	277.M	451.M	409.M	369.M	377.M	402.M	489.M	413.M	458.M	437.M	500.M	LSB
ASSOC ADDRESS (ALL CODES)	----	280	776	248	776	264	360	777	280	345	776	----	DEC
MAX(+) LINEARITY ERROR &	0.00	270.M	451.M	0.00	114.M	326.M	397.M	484.M	249.M	442.M	163.M	500.M	LSB
ASSOC ADDRESS (ABBREV)	----	282	776	777	456	776	361	776	793	379	328	----	DEC
MAX(-) LINEARITY ERROR &	-500.M	-205.M	-394.M	-358.M	-300.M	-284.M	-330.M	-448.M	-334.M	-413.M	-378.M	0.00	LSB
ASSOC ADDRESS (ALL CODES)	----	743	247	774	247	759	663	247	743	931	247	----	DEC
MAX(-) LINEARITY ERROR &	-500.M	-199.M	-170.M	268.M	230.M	-268.M	-72.7M	96.9M	-201.M	-411.M	96.6M	0.00	LSB
ASSOC ADDRESS (ABBREV)	----	741	759	204	775	247	199	647	230	898	931	----	DEC
MAX(+) LINEARITY ERROR &	0.00	249.M	479.M	392.M	376.M	356.M	376.M	525.M%	382.M	431.M	464.M	500.M	LSB
ASSOC ADDRESS (VREF=-10V)	----	280	776	248	776	776	360	776	280	89	776	----	DEC
MAX(-) LINEARITY ERROR &	-500.M	-190.M	-384.M	-325.M	-302.M	-272.M	-317.M	-433.M	-318.M	-373.M	-364.M	0.00	LSB
ASSOC ADDRESS (VREF=-10V)	----	743	247	775	247	759	662	247	742	903	247	----	DEC
MAX(+) LINEARITY ERROR &	0.00	243.M	445.M	373.M	366.M	337.M	389.M	523.M%	392.M	420.M	427.M	500.M	LSB
ASSOC ADDR (VREF=+1.25V)	----	280	776	507	776	264	361	777	280	346	776	----	DEC
MAX(-) LINEARITY ERROR &	-500.M	-185.M	-413.M	-303.M	-330.M	-312.M	-300.M	-461.M	-320.M	-348.M	-397.M	0.00	LSB
ASSOC ADDR (VREF=+1.25V)	----	741	247	517	247	759	695	247	740	677	247	----	DEC

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 5-10. Mfr. Code C Data at 25°C.

CMOS MULTIPLYING D/A CONVERTER DEVICE TYPE 1218 VREF = +10V EXCEPT WHERE SPECIFIED 1 LSB= 2.4480MV

06 MAR 81 14:57:00 VDD = 15.0 VOLTS TEMPERATURE = +25 DEGREES C

PARAMETER	LO-LIM	S/N 4	S/N 5	S/N 7	S/N 8	S/N 9		HI-LIM	UNITS
ICC - ALL INPUTS AT 0.0V	0.00	800.M	675.M	755.M	730.M	1.25	2.00		MA
ICC - ALL INPUTS AT 15.0V	0.00	665.M	625.M	730.M	670.M	740.M	2.00		MA
ICC - ALL INPUTS AT 0.8V	0.00	760.M	710.M	805.M	730.M	1.20	2.00		MA
ICC - ALL INPUTS AT 2.4V	0.00	375.M	360.M	420.M	390.M	440.M	2.00		MA
IREF(+)-ALL INPUTS AT 15V	500.M	660.M	620.M	645.M	620.M	620.M	2.00		MA
IREF(-)-ALL INPUTS AT 15V	-2.00	-650.M	-620.M	-655.M	-620.M	-635.M	-500.M		MA
IIL - ALL INPUTS AT 0.0V	-200.	PASS	PASS	PASS	PASS	PASS	1.00		UA
IIL - ALL INPUTS AT 0.8V	-200.	PASS	PASS	PASS	PASS	PASS	1.00		UA
IIH - ALL INPUTS AT 15.0V	-200.	PASS	PASS	PASS	PASS	PASS	1.00		UA
IIH - ALL INPUTS AT 2.4V	-1.00	FAIL	FAIL	FAIL	FAIL	FAIL	100.		UA
IZS - ALL INPUTS AT 0.0V	-200.	-160.	-160.	-160.	-160.	-160.	200.		NA
IZS' - ALL INPUTS AT 2.4V	-200.	-130.	-140.	-135.	-135.	-135.	200.		NA
dIZS/dT - INPUTS AT 0.0V	0.00	0.00	350.	21.3K	26.0K	0.00	0.00		PA/oC
dIZS'/dT- INPUTS AT 2.4V	0.00	0.00	100.	100.	100.	0.00	0.00		PA/oC
GAIN ERROR (VFS)	-100.	-1.92	-2.14	-4.25	-2.10	-1.97	100.		MV
GAIN ERROR (dVFS/dT)	0.00	0.00	0.00	0.00	0.00	0.00	0.00		PPM
PSS - VCC=15V TO 16V	-100.	-100.M	-350.M	650.M	150.M	300.M	100.		PPM
PSS - VCC=15V TO 14V	-100.	-150.M	50.0M	300.M	1.10	-1.05	100.		PPM
BIT LINEARITY ERROR - MSB	-500.M	179.M	36.6M	197.M	98.3M	50.3M	500.M		LSB
BIT LINEARITY ERROR - B2	-500.M	-37.3M	-13.1M	129.M	36.3M	85.0M	500.M		LSB
BIT LINEARITY ERROR - B3	-500.M	-48.2M	4.84M	-149.M	-29.7M	-3.00M	500.M		LSB
BIT LINEARITY ERROR - B4	-500.M	-126.M	-177.M	-121.M	-259.M	-206.M	500.M		LSB
BIT LINEARITY ERROR - B5	-500.M	3.05M	116.M	18.2M	173.M	75.3M	500.M		LSB
BIT LINEARITY ERROR - B6	-500.M	-7.59M	2.70M	-7.70M	-6.55M	121.M	500.M		LSB
BIT LINEARITY ERROR - B7	-500.M	27.9M	20.6M	-8.97M	-16.9M	33.4M	500.M		LSB
BIT LINEARITY ERROR - B8	-500.M	105.M	91.5M	55.1M	111.M	-24.8M	500.M		LSB
BIT LINEARITY ERROR - B9	-500.M	5.99M	-3.09M	-11.3M	-15.0M	13.5M	500.M		LSB
BIT LINEARITY ERROR - B10	-500.M	33.3M	33.6M	28.1M	22.3M	28.1M	500.M		LSB
BIT LINEARITY ERROR - B11	-500.M	39.1M	45.9M	42.0M	36.0M	40.4M	500.M		LSB
BIT LINEARITY ERROR - LSB	-500.M	38.9M	42.4M	42.4M	38.3M	43.8M	500.M		LSB
MAX(+) LINEARITY ERROR &	0.00	350.M	276.M	402.M	394.M	328.M	500.M		LSB
ASSOC ADDRESS (ALL CODES)	----	2099	2199	3089	3217	3303	----		DEC
MAX(+) LINEARITY ERROR &	0.00	322.M	238.M	390.M	381.M	328.M	500.M		LSB
ASSOC ADDRESS (ABBREV)	----	2111	3255	3095	3223	3303	----		DEC
MAX(-) LINEARITY ERROR &	-500.M	-309.M	-307.M	-385.M	-390.M	-257.M	0.00		LSB
ASSOC ADDRESS (ALL CODES)	----	1996	3945	1000	872	796	----		DEC
MAX(-) LINEARITY ERROR &	-500.M	-268.M	-272.M	-74.4M	-390.M	-254.M	0.00		LSB
ASSOC ADDRESS (ABBREV)	----	1888	3400	2668	872	792	----		DEC
MAX(+) LINEARITY ERROR &	0.00	0.00	0.00	0.00	0.00	0.00	500.M		LSB
ASSOC ADDRESS (VREF=-10V)	----	2025	360	1005	877	280	----		DEC
MAX(-) LINEARITY ERROR &	-500.M	-461.M	-481.M	-621.MX	-585.MX	-507.MX	0.00		LSB
ASSOC ADDRESS (VREF=-10V)	----	2071	2711	3089	3218	3783	----		DEC
MAX(+) LINEARITY ERROR &	0.00	288.M	249.M	312.M	294.M	231.M	500.M		LSB
ASSOC ADDR (VREF=+1.25V)	----	2103	183	3076	1175	71	----		DEC
MAX(-) LINEARITY ERROR &	-500.M	-467.M	-443.M	-589.MX	-552.MX	-516.MX	0.00		LSB
ASSOC ADDR (VREF=+1.25V)	----	1992	3428	1000	2412	8832	----		DEC

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

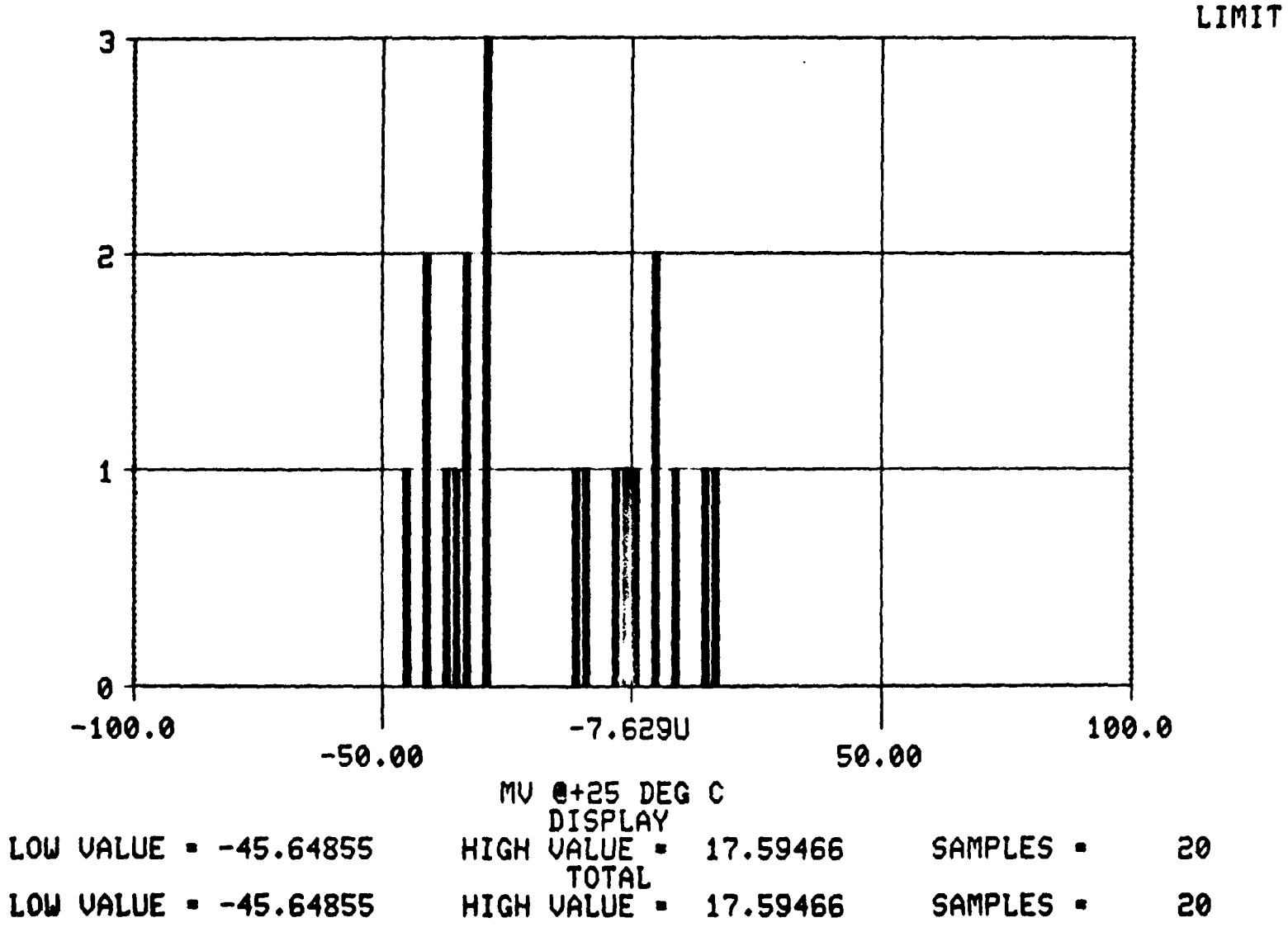


Figure 5-10. Histogram of Gain Error.

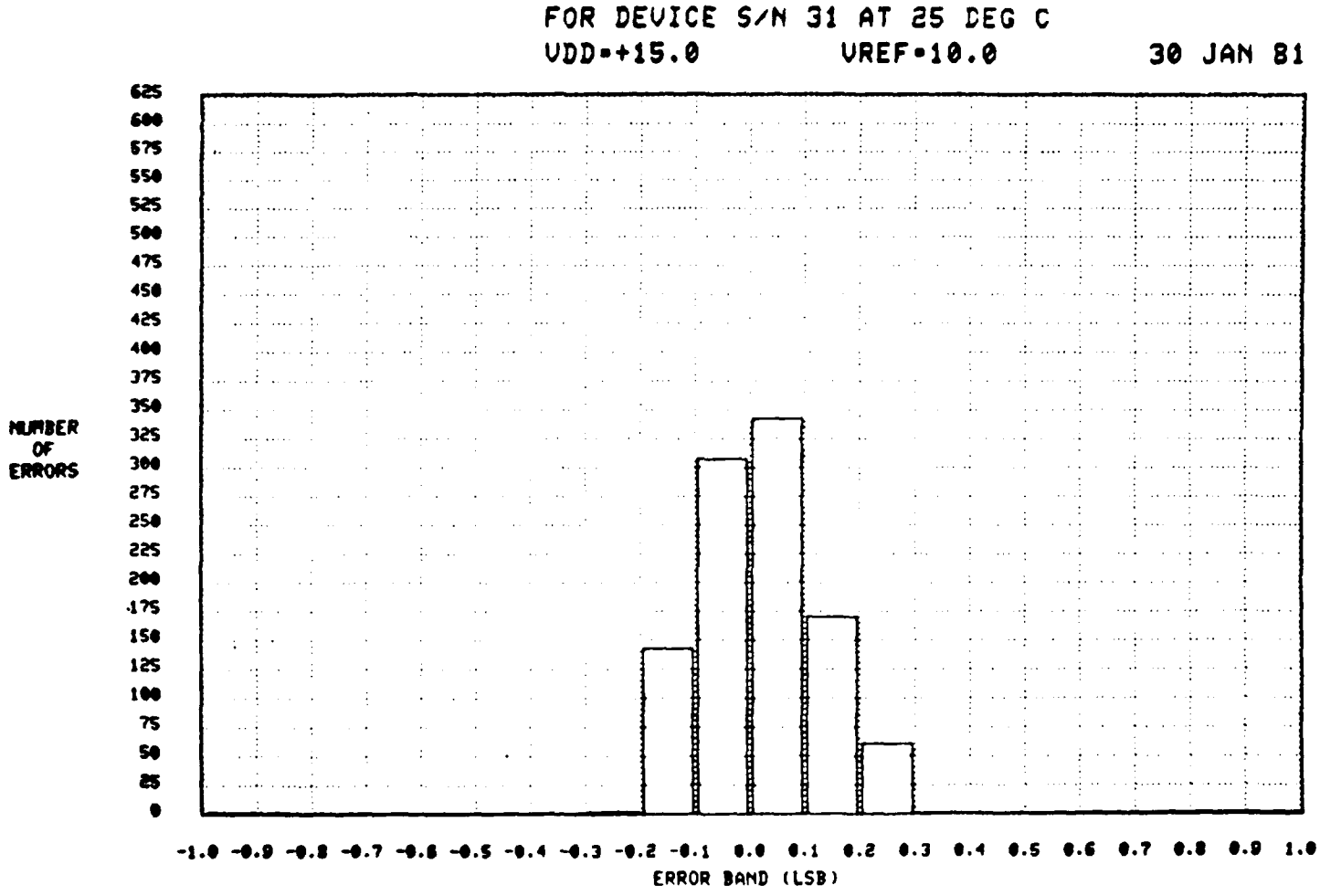


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Figure 5-11. Linearity Error Histogram.

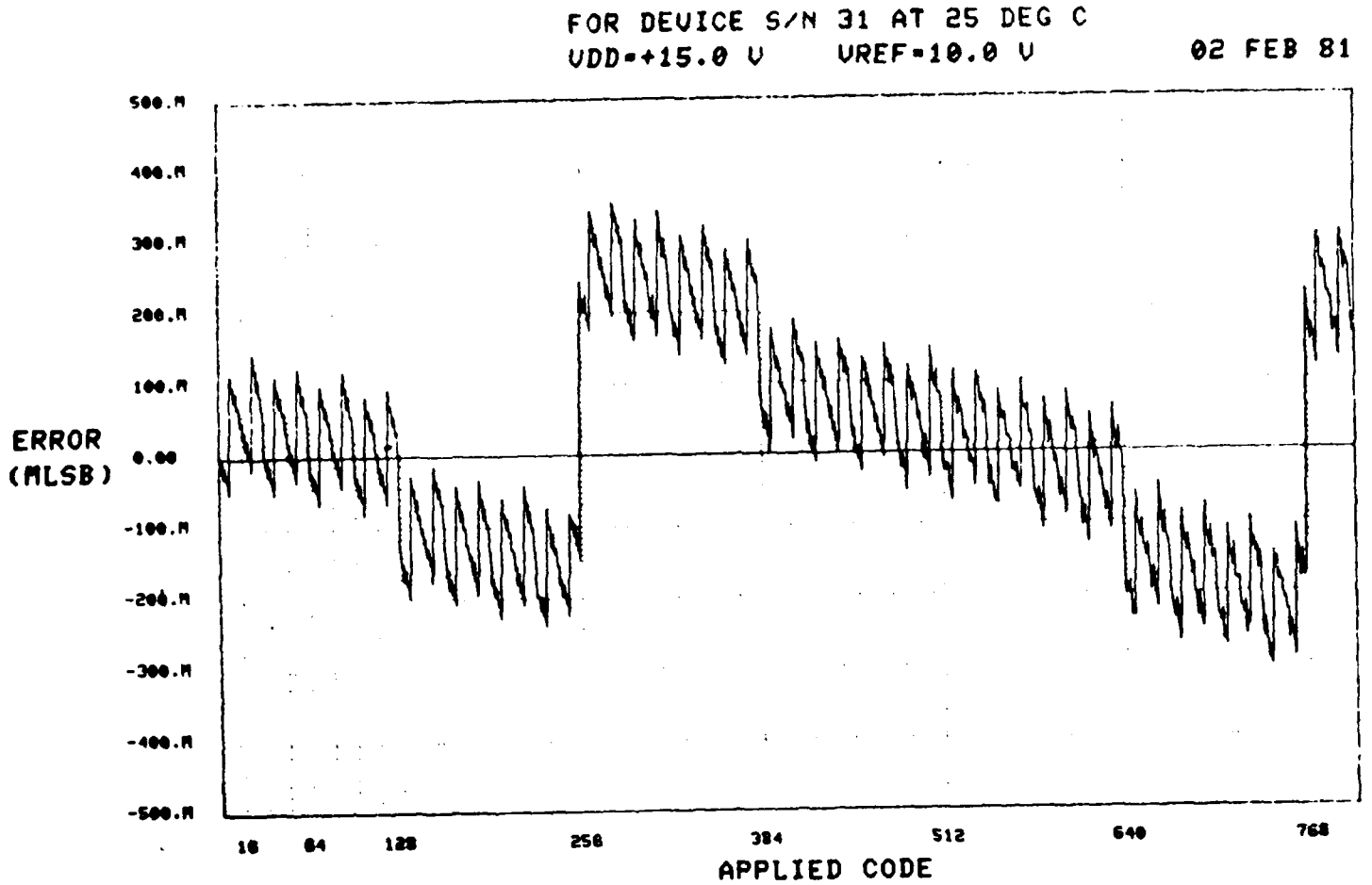
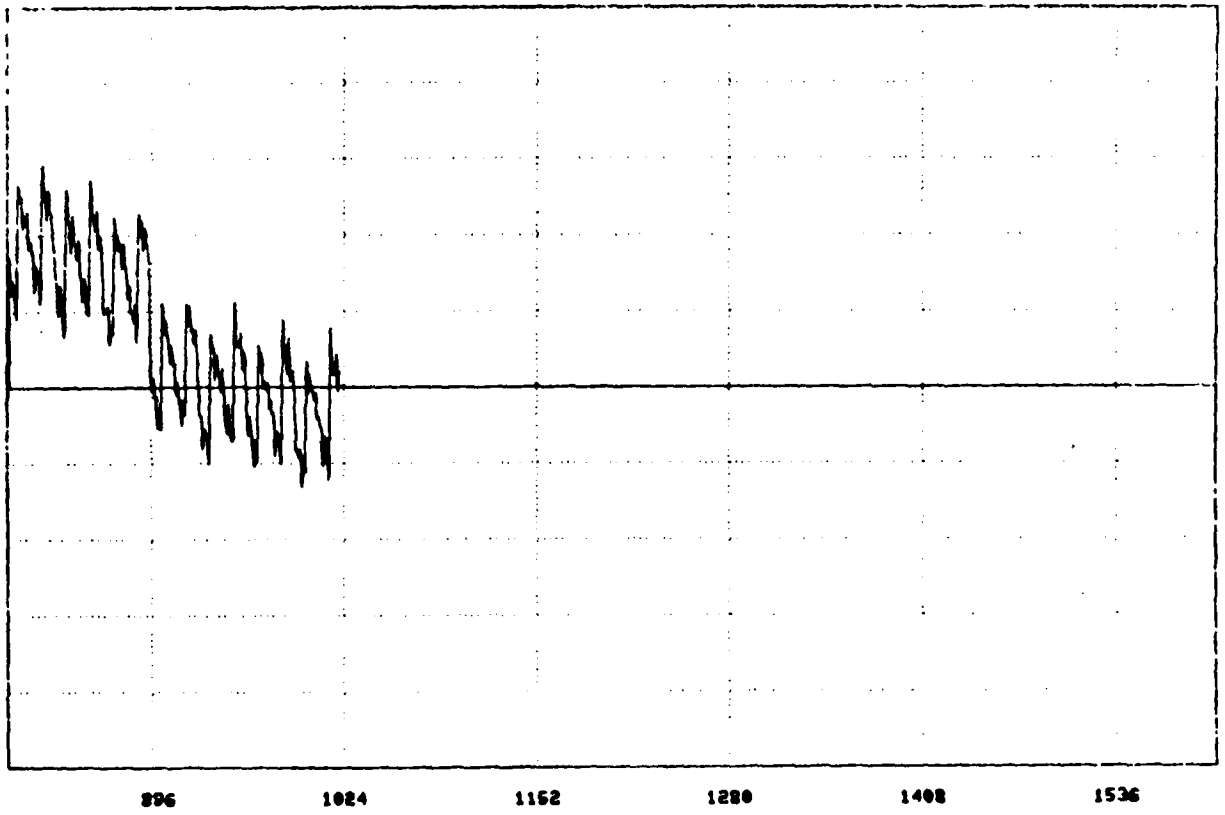


Figure 5-12. Linearity Error vs Input Code.

FOR DEVICE S/N 31 AT 25 DEG C
VDD=+15.0 V VREF=10.0 V 02 FEB 81



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WORST CASE POSITIVE BIT ERROR=
354.8MLSB @ ADDRESS 280

WORST CASE NEGATIVE BIT ERROR=
-304.5MLSB @ ADDRESS 743

Figure 5-12. Linearity Error vs Input Code. (cont.)

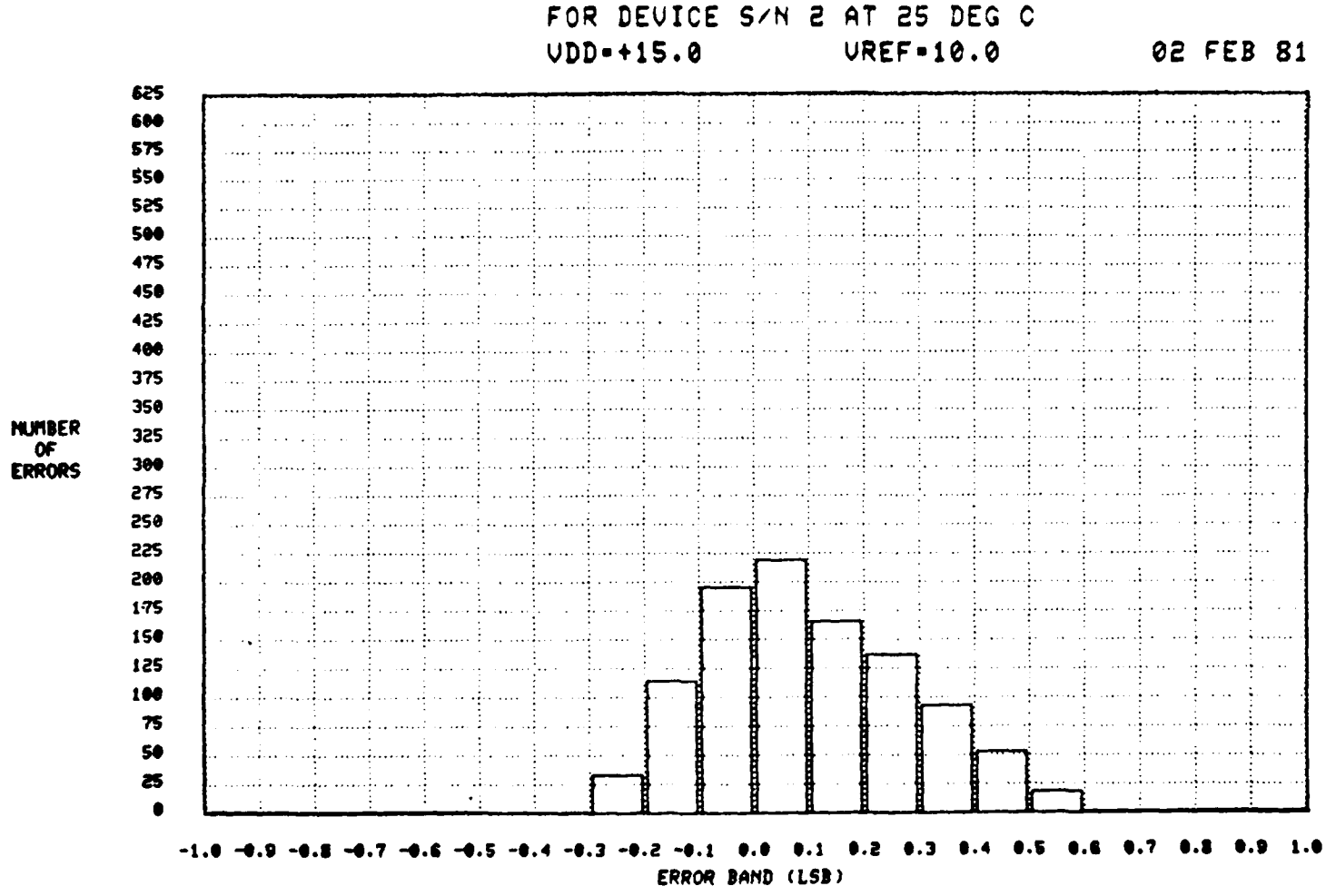

Figure 5-13. Linearity Histogram at VREF = + 10 V.

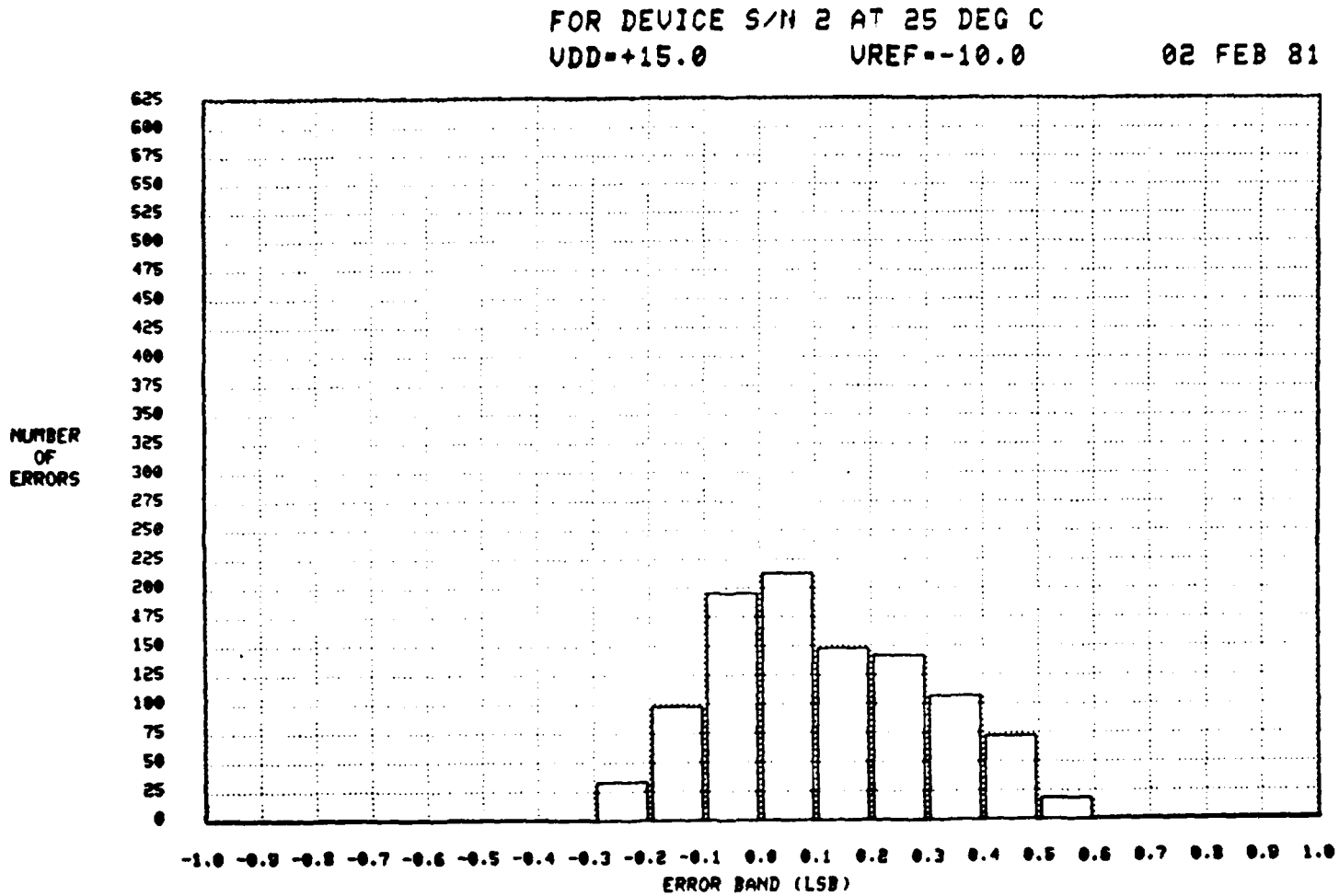

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Figure 5-14. Linearity Histogram at VREF = - 10 V.

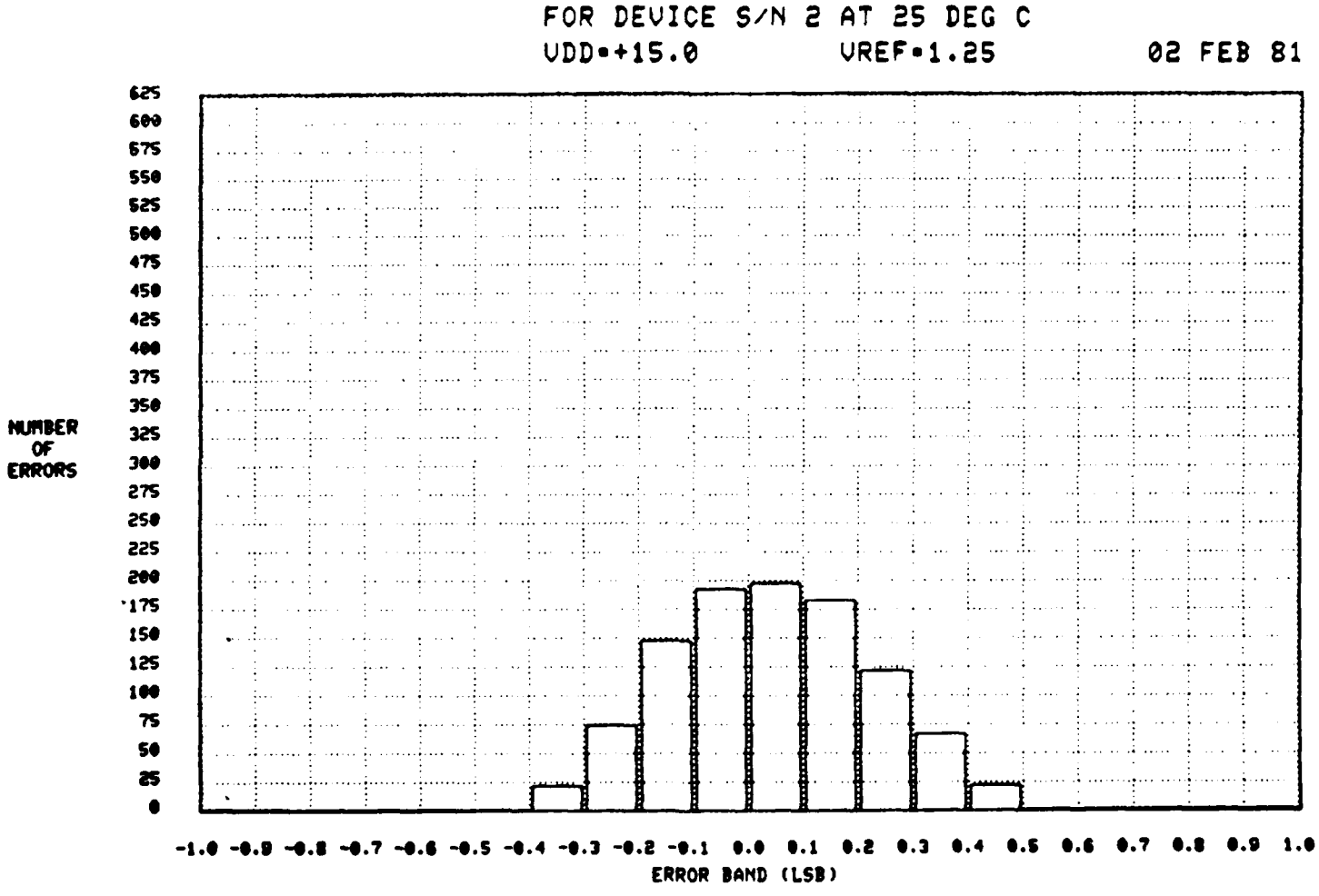

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Figure 5-15. Linearity Histogram at VREF = 1.25 V.

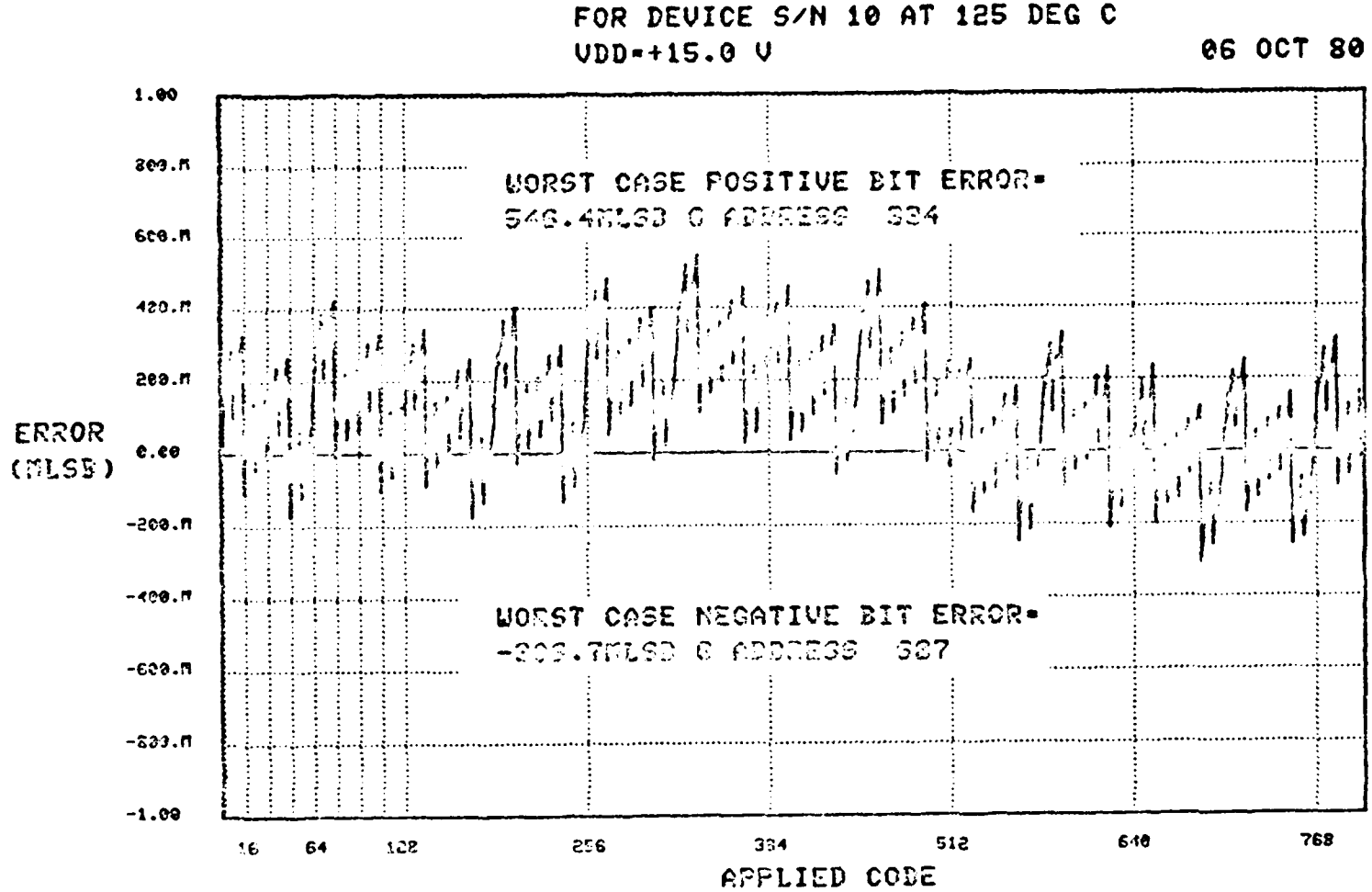

Figure 5-16. Linearity Plot at V_{CC} = + 15 V and T_A = 125°C for S/N 10.

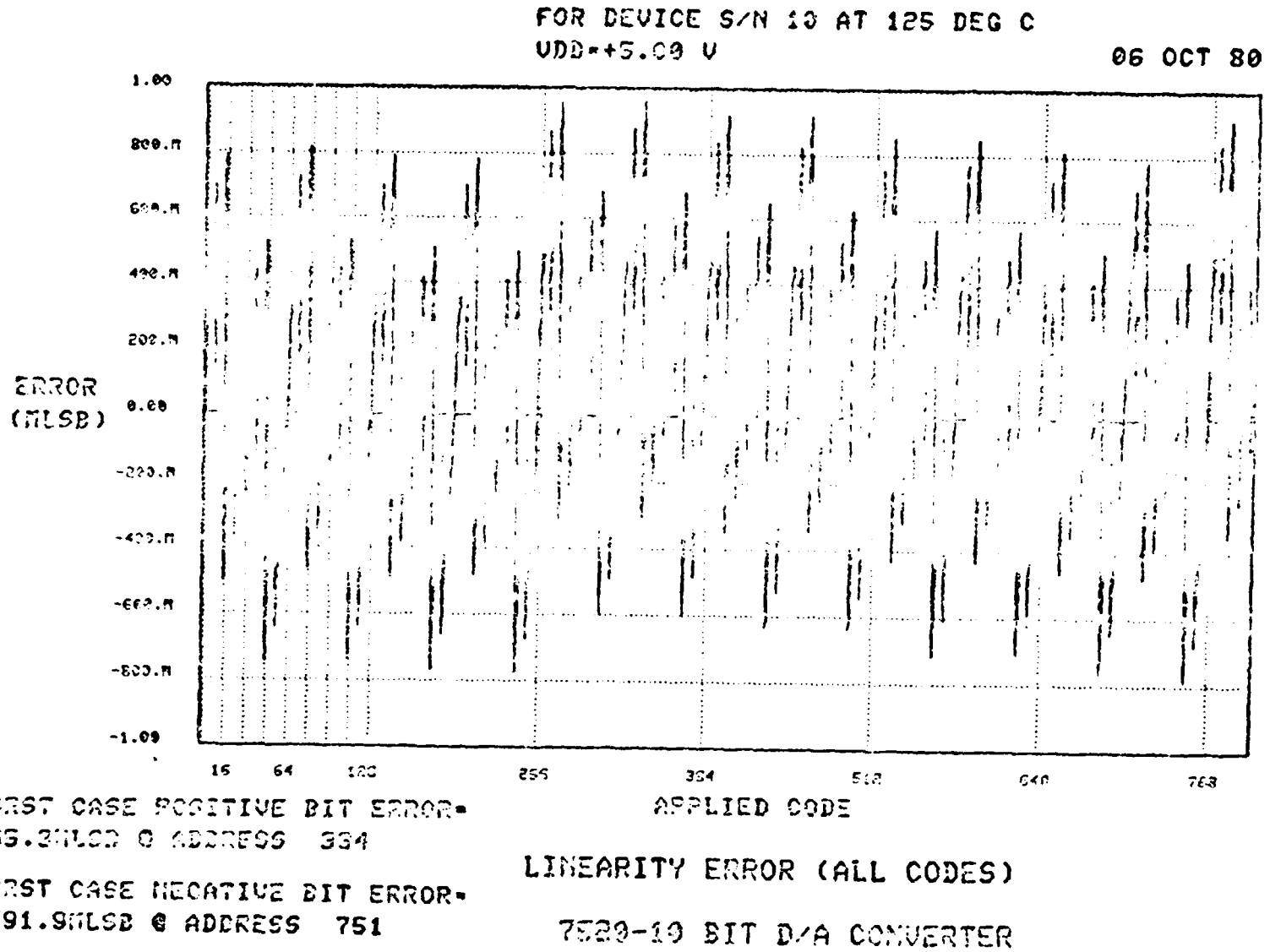

Figure 5-17. Linearity Plot at V_{cc} = + 5 V and T_A = 125°C for S/N 10.

Table I. Electrical performance characteristics. 1/

Characteristic	Symbol	Conditions: Vcc = + 15V, Vref = + 10V, paragraph 3.4 and Figure 7.	Device Type	Limits Min	Limits Max	Units
Supply current from Vcc	Icc	All digital inputs at 0V	All	-	100	uA
		All digital inputs at Vcc	All	-	100	uA
		All digital inputs at 0.8V	All	-	2	mA
		All digital inputs at 2.4V	All	-	2	mA
Reference input current	Iref	All digital inputs at Vcc, IOUT1 and IOUT2 grounded; Vref= 10V	All	0.5	2	mA
		Vref= -10V	All	-2	-0.5	mA
Digital input leakage current	IIL	All digital inputs at 0V	01-05	-1.0	1.0	uA
		All digital inputs at 0.8V	06-09	-200	1.0	uA
	IIH	All digital inputs at Vcc	01-05	-1.0	1.0	uA
		All digital inputs at 2.4V	06-09	-1.0	100	uA
Zero scale current	IZS	All digital inputs at 0.8V	All	-200	200	nA
	IZS'	All digital inputs at 2.4V	All	-200	200	nA
Zero scale current drift	dIZS/dT	All digital inputs at 0.8V	All	(later)		pA/°C
Full scale error	+dVFS	All digital inputs at Vcc, IOUT2 at 0V. Vref = +10V	All	-1	1	%VFS
	-dVFS	As above with Vref = -10V	All	-1	1	%VFS
Full scale error drift	dVFS/dT	Change in +dVFS from -25°C to 125°C and from 25°C to -55°C	All	-10	10	ppm VFS/°C
Power supply sensitivity at full scale from Vcc.	+PSS, -PSS	All digital inputs at Vcc; IOUT2 at 0V; VCC = + 14V to +16V; Measured at IOUT1 and Rf	All	-100	100	ppm VFS/V

Table I. Electrical performance characteristics. 1/ (continued)

Characteristic	Symbol	Conditions: Vcc = + 15V, Vref = + 10V, paragraph 3.4 and Figure 7.	Device Type	Limits Min	Limits Max	Units
Linearity error (end point) 2/	LE	Measure the following:	01	-0.2	0.2	%VFS
		1. All combinations of the most significant four bits with the lower order bits turned off.	02	-.05	.05	%VFS
		2. The individual lower bits with the most significant four bits turned off.	03	-.05	.05	%VFS
		3. The code word with the most positive combination of bits in groups 1 & 2 above.	04	-.012	.012	%VFS
		4. The code words derived from group 3 with all lower order bits complemented one at a time.	05	-.012	.012	%VFS
			06	-.05	.05	%VFS
		5. The code word with the most negative combination of bits in groups 1 and 2.	07	-.05	.05	%VFS
		6. The code words derived from group 5 with all lower order bits complemented one at a time.	08	-.012	.012	%VFS
		7. Groups 1 through 6 with Vref = -10V.	09	-.012	.012	%VFS
		8. Group 1 through 6 with Vref = 1.25V.				
		9. Group A sample - all code combinations of the digital input bits.				
Bit linearity errors (best fit)	LE (BF)	If any end point linearity tests fail, certain devices may be tested to a best fit criteria. The vendor shall specify the criteria (i.e. 3/4 or 7/8 scale adjustment) and repeat all of the linearity tests.	05, 09	-.012	.012	%VFS

Table I. Electrical performance characteristics. 1/ (continued)

Characteristic	Symbol	Conditions: Vcc = + 15V, Vref = + 10V, paragraph 3.4 and Figure 7.	Device Type	Limits Min	Limits Max	Units
Major carry errors (differential linearity)	MCE	The difference between adjacent codes at all major transitions. (i.e. from 01111111 to 10000000)	01	-0.4	0.4	%VFS
			02,03 06,07	-0.1	0.1	%VFS
			04,05 08,09	-.025	.025	%VFS
Feedthrough error	FTE	Vref=20Vpp, 100kHz and all digital inputs low. TA=25°C, Group D only. See Figure 8.	01-05	-	10	mVpp
			06-09	-	25	mVpp
Output current settling time (to 1/2 LSB)	tSLH	All inputs switched simultaneously, low to high and	All	-	1	usec
	tSHL	high to low . TA=25°C. See Figure 9. 3/	All	-	1	usec
Output capacitance	Co	All digital inputs at Vcc. See Figure 10. TA = 25°C. Co at IOUT1	All	-	200	pF
		Co at IOUT2	All	-	75	pF
Output capacitance	Co	All digital inputs at 0V. See Figure 10. TA = 25°C. Co at IOUT1	All	-	75	pF
		Co at IOUT2	All	-	200	pF
Noise	en	The single source of noise is the resistor network, which characteristically has Johnson or thermal noise. 4/	All	6.5	40	Kohm

Notes:

1/ See definitions as described in 6.5.

2/ Linearity is specified to be within +/- 1/2 LSB. Thus an 8 bit device with a 10V reference must have end point linearity to within 1/2 of (100%VFS/2exp8) = 0.195 %VFS or 0.2 %VFS.

3/ For each device type, output current settling time is the duration from the digital input transition until the output for a 10V analog input transition is within 1/2 LSB of final value.

4/ The R-2R resistor network has Johnson or thermal noise. Noise at the DUT output is related to the noise resistance value according to en = SQR(4KTRn(BW))
where K = Boltzmann's constant = 1.38*E-23 joules/°K
T = Absolute temperature in °K
Rn = Rf(1+Rf/Ro) changes with Ro and the digital code word
BW = Bandwidth in Hertz.

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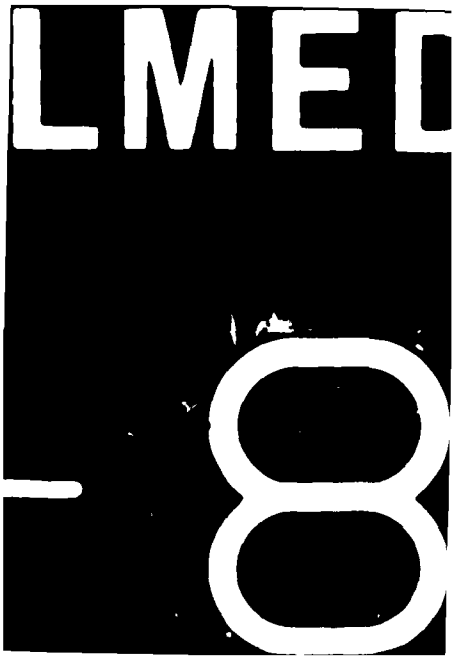
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